



19 OCT / MON

3F, Grand Hilai Taipei

Room	3F, Grand Hilai Taipei
9:30-9:50	Opening & Award Ceremony
9:50-10:40	Plenary Speech I Energy-Efficient AI Hardware - Beyond the Exit of the Device Miniaturization Tunnel Dr. H.-S. Philip Wong Willard R. and Inez Kerr Bell Professor Stanford University
10:40-11:30	Plenary Speech II Optimizing AI System with Advanced Packaging Dr. C.P. Hung Vice President of Corporate R&D ASE, Inc.
11:30-13:30	Lunch Break Lunch talk by Delta Air Lines
13:30-14:20	Plenary Speech III Advanced Semiconductor Package Substrates for AI and HPC Mr. Yasushi Araki Corporate Officer, GM of R&D Div. Shinko Electric Ind. Co., Ltd.
14:20-14:40	Coffee Break
14:40-17:40	S1 IAAC (IMAPS All Asia Conference) - Substrate Ecosystem and Growth: Scaling ABF, Glass, and High-Density IC Substrates for an AI-Driven World

20 OCT / TUE

7F, TaiNex 2

Room	701A						
9:00-9:50	Plenary Speech IV - Advanced Packaging Technologies for the AI era Dr. Rahul Manepalli, Vice President, Intel						
10:00-10:10	Break Time						
Room	701A	701B	701F	701G	701H	702	703
10:10-12:10	S2 Enable Energy-Efficient AI Technologies Through Integrated Material Solutions (Qnity)	S3 Compute & Enterprise AI (AMD)	S4 Advanced Packaging ~ Hybrid bonding, Glass core, Fine RDL ~ (ICEP)	S5 Signal, Power and RF Integrity	S6 Advanced Testing and High-Speed Characterization	S7 Advanced Interconnect Technologies	S8 Advanced Package Design and Performance
12:10-13:00	Lunch Break / Lunch talk by Resonac @ 701A						
13:00-15:00	S9 Glass substrate	S10 Advancements in Components to System Integration (GEA)	S11 Architecting the Future: AI-Driven Data Center Systems (intel)	S12 Advanced RDL and Fan-Out Technologies for Next-Generation Packaging	S13 AI-Driven Advanced Packaging	S14 Advanced Bonding Technologies	S15 Copper Metallization and Surface Finishing
15:00-15:50	Poster session I /Coffee Break @ 701E						
15:50-17:50	S16 Next-Generation AI Server & Advanced Liquid Cooling (TTMA)	S17 Surround the Glass-Advanced Packaging transition to Glass Core Substrate (MKS' Atotech)	S18 Thinking Big: How Panel-Level Packaging Is Reshaping Heterogeneous Integration (Applied Materials)	S19 Hybrid Bonding for 3D Integration	S20 Design, Test and Reliability	S21 Advanced Materials and Assembly Technologies	S22 Sustainable Electronics and Emerging Technologies

21 OCT / WED

7F, TaiNex 2

Room	701A						
9:00-9:50	Plenary Speech V - Effects of Aging, Damage, and Crystal Orientation on the Reliability of Solder Joints for Advanced Packaging and Heterogeneous Integration Dr. Jeffrey C. Suhling, Quina Distinguished Professor, Auburn University/ President, IEEE-EPS						
10:00-10:10	Break Time						
Room	701A	701B	701F	701G	701H	702	703
10:10-12:10	S23 Advanced Package in AI Era (ASE)	S24 Building the AI Packaging Ecosystem Innovations in Research, Materials, Equipment & Manufacturing (Lam Research)	S25 Glass Technologies for Advanced Packaging	S26 Power Electronics Packaging		S27 Interconnection Materials and Assembly	S28 High-Speed AI and Data Center PCB Technology
12:10-13:00	Lunch Break / Lunch talk by Paeonia @ 701A						
13:00-15:00	S29 Heterogeneous Integration in Advanced Packaging (SPIL)	S30 Advanced Glass and Interposer Technologies for Heterogeneous Integration (Hi-CHIP)	S31 Advanced Packaging Process Technologies	S32 Package Mechanics and Reliability	S33 Design, Modeling and Simulation	S34 Thermal Characterization and Management	S35 Advanced Substrate and Packaging Materials
15:00-15:50	Poster session I /Coffee Break @ 701E						
15:50-17:50	S36 Heterogeneous Integration	S37 Thermal Management and Interposer Materials for Advanced Semiconductor Packaging (ISMP)	S38 Addressing high power consuming systems: Materials & processes research in Japan (JIEP)	S39 Advanced Packaging Manufacturing & Processing	S40 Modeling and Reliability of Advanced Packaging		S41 Smart Manufacturing, Inspection and Testing

**Energy-Efficient AI:
From Computing to Systems
and Applications**

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22 OCT / THU

4F, TaiNEX 1

Time	Program	
10:00-12:00	PDC 1 Co-Packaged Optics (CPO) with Silicon Photonics: Heterogeneous Integration of Chiplets in Switch ASIC, Photonic IC (PIC), and Electronic IC (EIC) and Glass Packaging - Dr. John Lau	Room 402bc
10:00-12:00	PDC 2 High Reliability Soldering in Advanced Semiconductor Packaging - Dr. Ning-Cheng Lee	Room 403

OPEN SEMINAR TPCA Show Main Stage (L-1409)

4F, TaiNEX 1

Date	Time	TOPIC
20 OCT. TUE	14:00-16:00	Open Seminar I Market trend - SiPh/CPO Heterogeneous Integration in the AI Era: CoPoS × TGV (TPCA)
21 OCT. WED	15:10-16:50	Open Seminar II Large Form Factor Assembly (iNEMI)
22 OCT. THU	13:00-14:00	Open Seminar III IEEE-EPS Distinguished Lecture Dr. John Lau