

Final Program

IMPACT 2024
International Microsystems, Packaging,
Assembly and Circuits Technology conference

October 22nd(Tue)- 25th(Fri), 2024
Taipei Nangang Exhibition Center



19th International Microsystems,
Packaging, Assembly and Circuits Technology Conference



台灣國際微電子
暨構裝學會



ITRI
Industrial Technology
Research Institute

TPCA 台灣電路板協會
Taiwan Printed Circuit Association



IMPACT Official Site



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TUE October 22					
Venue	R504a				
13:00-14:00	IEEE-EPS Distinguished Lecture - Dr. John Lau				
Venue	R504a		R504b		
14:30-17:40	Professional Development Course 1 Dr. John Lau		Professional Development Course 2 Dr. Ning-Cheng Lee		

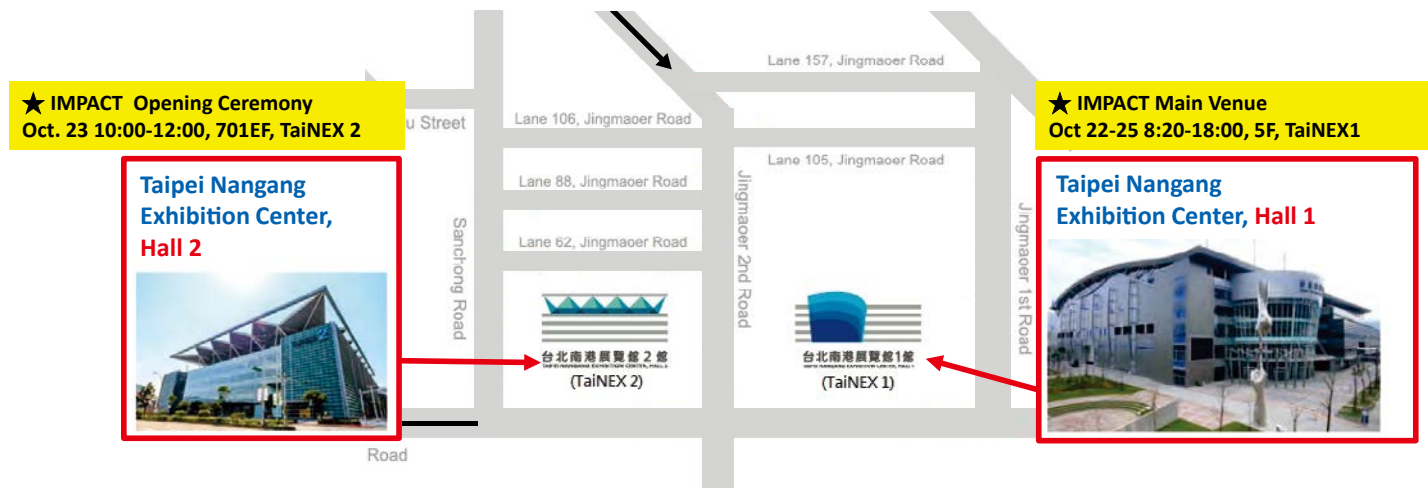
WED October 23					
Venue	Room 701 EF, TaiNEX 2				
10:00-10:20	Opening & Award Ceremony				
10:20-11:10	Plenary Speech I : PEC Technology Evolution in IOWN for More than Moore Hidehiro Tsukano, Senior Vice President, NTT				
11:10-12:00	Plenary Speech II : Specialty Technology Dr. C.S. Yoo, Vice President , TSMC				
12:00-13:30	Lunch Break				
Venue	R504a	R504b	R504c	R503	R502
13:30-15:30	【 S1 】 Ecosystem Enabling for Intel Data Center AI Server Solutions (Intel)	【 S2 】 Advancing AI chips from silicon to PCB (MKS' Atotech)	【 S3 】 Advanced Packaging Technologies-1	【 S4 】 Design, Modeling, AI/ Machine Learning Applications, and Testing -1	【 S5 】 Sustainable Technologies & Systems
15:00-16:00	Poster Session I (Happy Hour 15:20-16:00)				
16:00-18:00	【 S6 】 Server Solution Customer SI+EV Enablement (AMD)	【 S7 】 Topics for advanced packaging processes in Japan (JIEP)	【 S8 】 Advanced Packaging Technologies-2	【 S9 】 HDI, IC Substrate and FPC Technology-1	【 S10 】 Power Electronics Packaging-1
17:50-20:00	TPCA Show & IMPACT Joint Reception				

THUR October 24					
Venue	Room 504, TaiNEX 1				
9:00-9:50	Plenary Speech III : Advanced Packaging Technologies in Memory Applications for AI Era Ki III Moon, Vice President, SK Hynix				
9:50-10:40	Plenary Speech IV : Heterogeneous Integration for Edge Applications Glenn Daves, Senior Vice President, NXP				
10:40-12:10	【 S11 】 IEEE EPS Panel, Heterogeneous Integration Roadmap Compact Session (ASE)				
12:00-13:30	Lunch Break				
Venue	R504 a	R504 b	R504 c	R503	R502
13:30-15:30	【 S12 】 Shaping Our Future with AI by Next-Gen Substrate and Packaging (Dupont)	【 S13 】 Market trend-Innovative 3D IC Heterogeneous Integration Packaging	【 S14 】 ICEP	【 S15 】 Advanced Packaging Technologies-3	【 S16 】 Design, Modeling, AI/ Machine Learning Applications, and Testing -2
15:00-16:00	Poster Session II (Happy Hour 15:20-16:00)				
16:00-18:00	【 S17 】 Advanced Packaging (SPIL)	【 S18 】 SMTA	【 S19 】 Power Electronics Packaging-2	【 S20 】 Advanced and Green Materials and Process-1	【 S21 】 Test, Quality, Inspection and Reliability / Simulation
18:00-20:00	IMPACT Welcome Dinner (By Invited ONLY)				

FRI October 25					
Venue	R504 a	R504 b	R504 c	R503	R502
8:20-10:20	【 S22 】 ISMP	【 S23 】 Glass Substrate	【 S24 】 Interconnections & Nanotechnology	【 S25 】 HDI, IC Substrate and FPC Technology-2	【 S26 】 Advanced Materials, Automatic Process & Assembly
10:30-12:30	【 S27 】 Heterogeneous Integration	【 S28 】 Advanced Packaging Technologies-4	【 S29 】 Design, Modeling, AI/Machine Learning Applications, and Testing / Smart manufacturing	【 S30 】 Advanced and Green Materials and Process-2	【 S31 】 Test, Quality, Inspection and Reliability / Smart Manufacturing
12:30-13:30	Lunch Break				
13:30-15:30	【 S32 】 3D embedding technology toward heterogeneous integration	【 S33 】 Design, Modeling, AI/Machine Learning Applications, and Testing /Advanced Process	【 S34 】 Interconnections & Nanotechnology & Advanced Materials, Automatic Process & Assembly	Plenary Speech	Industrial / Special Session
				Packaging Session	PCB Session
				Poster Session	Special Event

*The organizer reserves the right to modify the agenda.

Floor Plan



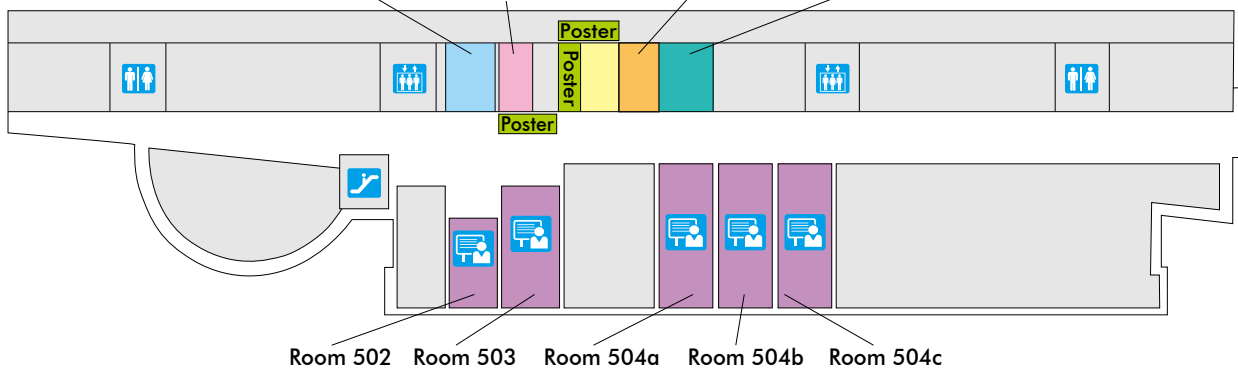
IMPACT 2024

Speaker Preview Room Organizer's Office Registration VIP Lounge



Conference Room

WIFI for 5F



5_F

4_F

TPCA Show — TAIPEI —

3_F



1_F

Index

Conference Agenda	Inside Cover
Organizer, Co-Organizer and Sponsor	1
Greeting of Chair	
Welcome Message from Shen-Li Fu, Conference General Chair	3
Welcome Message from Kuo-Ning Chiang, Conference Honorary Chair	4
Welcome Message from Shih-Chieh Chang, Conference Co-Chair	5
Welcome Message from Shin-Puu Jeng, Conference Co-Chair	6
Welcome Message from Scott Chen, Conference Co-Chair	7
Committee Member	8
General Information	
About Conference	13
TPCA Show /Welcome Dinner /IMPACT Best Paper 2023/Identification Badge / Registration Desk / Organizer's Office & Speaker Preview Room / Poster Session / Internet Access / Hotel Information /Guideline for health and safety /Inquiries	13-17
Conference	
Plenary Speeches	18
Sessions	22
Poster session I - Packaging	56
Poster session II - Packaging & PCB	58
Note	60
IMPACT Sponsor	
AMD	63
Applied Material	64
ASE	65
Dupont	66
Intel	67
MKS' Atotech	68
SPIL	69
Lam / Omron	70
Pre-Announcement- IMPACT 2025	Inside Back Cover

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Co-Organizer



Industrial / Special Session



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Welcome Message from Shen-Li Fu, Conference Chair



Shen-Li Fu
Chair of IMPACT 2024
Chair, IEEE EPS – Taipei
Honorary President, I-Shou University

On behalf of the IMPACT 2024 Organizing Committee, it is my great pleasure and honor to formally welcome you to the **2024 International Microsystems, Packaging, Assembly and Circuit Technology Conference (IMPACT 2024)**.

IMPACT 2024 Conference, which is organized by IEEE-EPS-Taipei, iMAPS-Taiwan, ITRI, and TPCA, is the largest gathering of **PCB** and **packaging** professionals in Taiwan. This year will be held on Oct. 22nd-25th at Taipei Nangang Exhibition Center, in conjunction with TPCA Show 2024. For grasping the latest trend, the symposium will focus on the theme "**IMPACT on Sustainable Technology**", which will explore the latest electronic technologies and fostering collaboration among enterprises and organizations.

This conference also collaborates with international organizations such as ICEP and JIEP from Japan, iNEMI and IEEE EPS from the USA, and global consulting companies like Yole Développement and Techsearch from the USA. Join us at IMPACT 2024 to be part of the future of electronic technology!

Best regards,



Shen-Li Fu, Ph.D.
Chair of IMPACT 2024
Honorary President, I-Shou University



Welcome Message from K. N. Chiang, Conference Honorary Chair



Kuo-Ning Chiang, Ph. D.

NTHU Chair Professor

Academician, International Academy of Engineering (IAE)

Fellow, IEEE / STAM / ASME / iMAPS / AIIA

Distinguishes Research Fellow, National Science and Technology Council

As the honorary chair of IMPACT2024, I am pleased to welcome participants worldwide to our annual event in Taipei. This gathering is an opportunity for us to share experiences and collaborate on advancements in microsystems, circuits, packaging, and PCBs over the next few days. IMPACT is recognized as one of the leading electronic packaging conferences, attracting over 500 attendees and featuring 200+ presented papers alongside the large TPCA exhibition each year.

IMPACT 2024 presents a robust program highlighting this year's latest trends and emerging technologies in electronic packaging and PCB sectors. The program will explore crucial topics, including Chiplets and heterogeneous integration, 3D/system-in-package (SiP), fan-out technologies, automotive applications, high-performance computing, 3AI/machine learning applications, and design-on-simulation technology. This conference will be an excellent platform for sharing knowledge, discovering emerging packaging trends, and exchanging innovative research ideas.

I hope you enjoy the program and the networking opportunities over the next few days. I am wishing you great success at this important conference. Thank you for your participation!

Best Wishes,

A handwritten signature in black ink that reads "knchiang". The signature is stylized, with the first letters of the first and last names being capitalized and prominent.

Kuo-Ning Chiang, Ph. D.

Honorary Chair of IMPACT 2024

Chair Professor, National Tsing Hua University

IMPACT Welcome Message from Shih-Chieh Chang, Conference Co-Chair



Shih-Chieh Chang, Ph.D.
Co-Chair of IMPACT 2024
General Director, ITRI

Dear Experts, Colleagues and Friends,

As a Co-Chair of the IMPACT 2024 committee, it is my great pleasure to warmly welcome all participants to this year's conference.

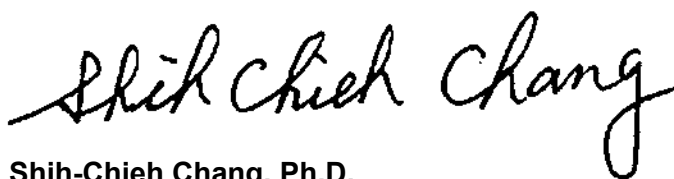
Under the theme of IMPACT on Sustainable Technology, we will delve into advanced microelectronic packaging and PCB technologies, focusing on the latest trends, challenges, and breakthroughs in this field. We are privileged to have leading experts from industry giants such as NTT, SK hynix Inc., NXP, TSMC, Unimicron, and ShinePure Hi-Tech, who will share their cutting-edge research and insights. I hope this platform will foster cross-disciplinary collaboration, ignite new ideas, and drive progress in both technology and sustainability.

The exciting program is carefully crafted by our Technical Program Committee, in conjunction with the professional teams of IEEE-EPS-Taipei, iMAPS-Taiwan, ITRI, and TPCA, to include plenary speeches, special sessions, and sponsored industrial sessions, complemented by exceptional paper and poster presentations.

I extend my sincere appreciation to all of you for taking time out of your busy schedule to attend this significant gathering. At the same time, we sincerely invite you to take this opportunity to visit at the city of Taipei. Taipei boasts a diverse array of cultural landmarks, exquisite cuisine, and an efficient transportation system, all of which are sure to leave a lasting impression on you. We look forward to sharing the unique charm of Taipei with you and experiencing the warmth and vibrancy of this city together.

Thank you all once again for joining us today and wish everyone great success for this event. Thank you!

Sincerely,



Shih-Chieh Chang, Ph.D.
Co-Chair of IMPACT 2024
General Director, ITRI



Welcome Message from Shin-Puu Jeng, Conference Co-Chair



Shin-Puu Jeng
Co-Chair of IMPACT 2024
President, IMAPS-Taiwan

Dear Colleagues and Friends,

As the Conference Co-Chair of the 2024 IMPACT Conference, it is my pleasure to welcome you to this significant annual event—the 19th International Microsystems, Packaging, Assembly and Circuits Technology Conference. This year, we focus on a vital theme: Sustainable Technology.

In our rapidly evolving landscape, the call for sustainable solutions has never been more urgent. As we embrace new frontiers in technology, it is imperative that we prioritize sustainability in our innovations. This conference serves as a platform to explore how we can integrate sustainable practices into our work, particularly within the realms of semiconductor technology and electronic packaging.

The advancements in sustainable technology are not just beneficial—they are essential. They empower us to reimagine our approach to high-performance computing, artificial intelligence, and beyond. The innovations we discuss here are the backbone of the digital revolution, transforming everything from everyday devices to sophisticated AI systems and autonomous vehicles.

At the heart of this transformation is advanced electronic packaging. By fostering heterogeneous integration, we are breaking barriers and enabling seamless connections among various components and materials. This is where the magic happens—where innovation meets sustainability, driving us toward a more efficient and eco-friendly future.

This conference is designed to bring together professionals from industry, research, and academia to engage in meaningful discussions about emerging trends, technologies, and the challenges we face. I encourage each of you to seize this opportunity to forge new connections, share insights, and collaborate on ideas that will shape the future of our field.

Thank you for being part of this incredible journey of discovery and collaboration. I wish you all an inspiring and enriching experience during our time together at IMPACT 2024.

Let's work together to make a lasting impact!

Best Wishes,

Shin-Puu Jeng, Ph.D
Co-Chair of 2024 IMPACT Conference
President, IMAPS-Taiwan

Welcome Message from Scott Chen, Conference Co-Chair



Scott Chen
Co-Chair of IMPACT 2024
Vice Chairman,TPCA
CEO, Kinsus Interconnect Technology Corp.

It is my honor and privilege to welcome you to IMPACT 2024, a global platform where innovators and thought leaders from the electronics, packaging, and PCB industries converge to explore the latest advancements and future directions. This year's theme, "IMPACT on Sustainable Technology", emphasizes the indispensable role that sustainability plays in driving technological progress, particularly in the advanced development of both the Packaging and PCB sectors. The integration of these two fields is shaping the future of electronics, enabling the creation of smarter, more efficient, and eco-friendly systems.

At IMPACT 2024, we are excited to present a diverse array of sessions dedicated to cutting-edge technologies, such as high-density interconnects, advanced packaging, glass substrates, and sustainable materials in PCB manufacturing. These sessions will underscore the critical synergy between packaging and PCB innovations—demonstrating how their combined advancements are not only overcoming today's technical challenges but also laying the foundation for a future where sustainability permeates every aspect of the manufacturing process. From AI applications to electric vehicles, the collaborative contributions of the packaging and PCB industries are crucial to realizing a sustainable, digitally connected world.

We invite you to actively engage, collaborate, and explore the vast opportunities presented at this year's conference. Together, we can push the boundaries of innovation and sustainability, and I look forward to witnessing the valuable exchanges that will shape the future of our dynamic industries.

Best Regards,



Scott Chen
Co-Chair of IMPACT 2024
Vice Chairman,TPCA
CEO, Kinsus Interconnect Technology Corp.



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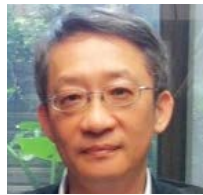
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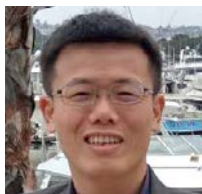
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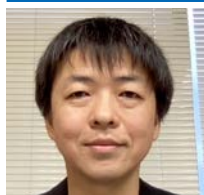


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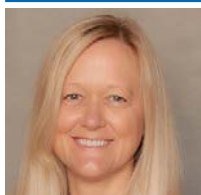
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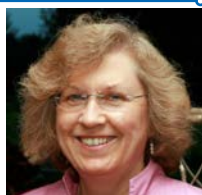


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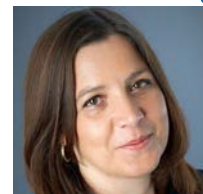
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General Information of IMPACT 2024

Join us at IMPACT 2024, the premier conference for PCB and packaging professionals in Taiwan, organized by IEEE-EPS-Taipei, iMAPS-Taiwan, ITRI, and TPCA. This year's event will be held from Oct. 22nd-25th at Taipei Nangang Exhibition Center, in conjunction with TPCA Show 2024. The symposium will focus on the theme "IMPACT on Sustainable Technology", exploring the latest electronic technologies and fostering collaboration among enterprises and organizations.

As artificial intelligence, quantum computing, and low-earth orbit satellite communications rapidly advance, the convergence of technology and resource sustainability becomes an increasingly urgent strategic imperative. IMPACT 2024 will delve into these technological innovations and sustainability advancements in PCB and packaging, offering professional development courses, plenary speeches, special sessions, industrial sessions, invited talks, outstanding papers, and poster presentations.

This conference also collaborates with international organizations such as ICEP and JIEP from Japan, IEEE EPS, iNEMI, SMTA from the USA, ISMP from South Korea, and global consulting companies like Techsearch from the USA. Join us at IMPACT 2024 to be part of the future of electronics technology!

We are pleased to bring you the annual technology gala of packaging, microsystems, assembly, PCB, materials, and thermal. Hope you can enjoy the over 250 papers, speeches, posters and discussions. We sincerely pledge this conference can bring you access to meet industrial best practices, create an opportunity for networking, and build international collaborations.

About Conference

- **Date:** October 22(Tue) – October 25 (Fri), 2024
- **Venue:** Taipei Nangang Exhibition Center, Taipei (TaiNEX)
- **Exhibition :** TPCA Show 、TAITRONICS 、AIoT Taiwan
- **Theme:** IMPACT 2024 on Sustainable Technology

Registration Desk

Please check in and get badge & conference materials as following times

Opening Ceremony

10/23 09:00-11:20, 7F, TaiNEX 2

Main Registration

10/23 11:00-16:30, 5F, TaiNEX 1

10/24 08:30-16:30, 5F, TaiNEX 1

10/25 08:00-14:30, 5F, TaiNEX 1

Organizer Office & Speaker Preview Room

For ORAL presenter, please do arrive at the Preview Room before your presentation to store your ppt files.

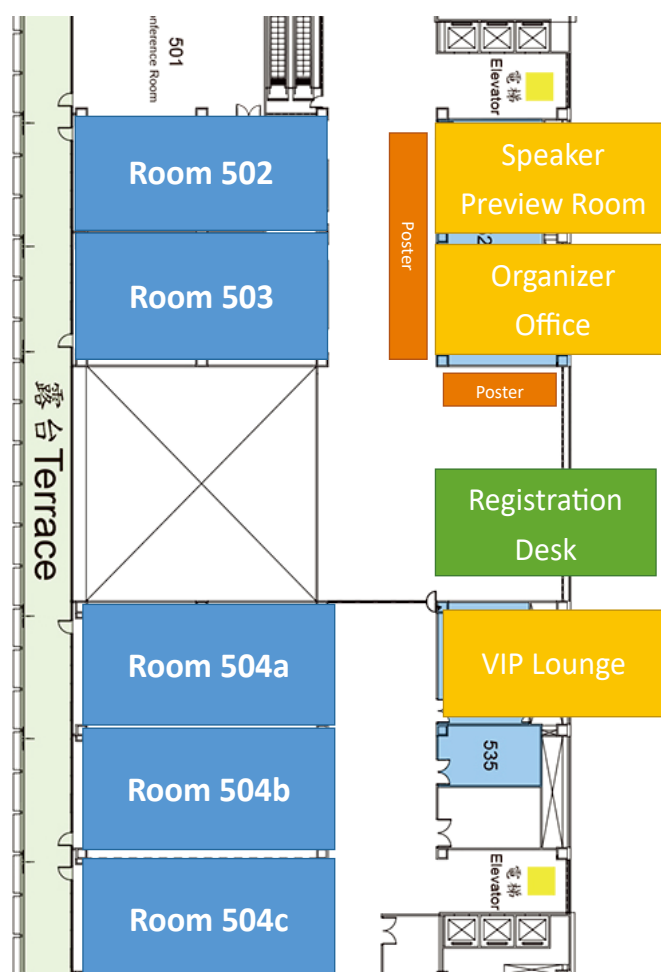
Location: 5F, TaiNEX 1

Open Hour:

10/23 10:00-17:30

10/24 08:30-17:30

10/25 08:00-15:00



Poster Session

For POSTER presenter, please display & stand by your poster during your presentation time

Location: Foryer Area, 5F, TaiNEX 1

Date/Time:

Poster Session I –15:00-16:00, Oct. 23rd, 2024

Poster Session II –15:00-16:00, Oct. 24th, 2024

Happy Hour will be served during the poster session from 15:20-16:00

Join us for networking and signature snacks

Lunch

Date/Time: 11:30-13:30, Oct. 23-25, 2024

Location: 3rd floor TaiNEX 1

Options : The Menu (Eastern style) OR Festival(Western style)

Access: VIPs (including Plenary Speakers, Invited Speakers, Session Chair, and Committee Members) as well as attendees who have paid for the lunch.

****Lunch Voucher is provided upon registration****

Internet Access

Wireless internet is provided on 5th floor of Taipei Nangang Exhibition Center for free.

TPCA Show & IMPACT Joint Reception

Time: Oct. 23, 2024 (17:50 – 20:00)

Venue: 3F Ballroom, Grand Hi-Lai Hotel, Taipei
(台北漢來大飯店3樓宴會廳)

Address: NO. 168, JINGMAO 1ST RD., NANGANG DIST.,
TAIPEI CITY 115, TAIWAN (台北市南港區經貿一路168號)

TEL: (02) 2788-6868

Access: Open to all. Please bring your badge for entry

Welcome Dinner (By invitation only)

Time: Oct. 24, 2024 (18:00 – 20:30)

Venue: 3F Ballroom, Grand Hi-Lai Hotel, Taipei
(台北漢來大飯店3樓宴會廳)

Address: NO. 168, JINGMAO 1ST RD., NANGANG DIST.,
TAIPEI CITY 115, TAIWAN
(台北市南港區經貿一路168號)

TEL: (02) 2788-6868

Access: Open to invited guests (Plenary Speakers, Invited speakers, Sponsors, VIP, Committee members)

Identification of Badges

Badges are required for admittance to all sessions and access to TPCA Show. Please bring it with you all the time.

Conference Venue Map



Contact: Ms. Cindy Lee / Tel: +886-3- 3815659#407 / Email: service@impact.org.tw

IMPACT Best Paper 2023

IMPACT 2023 received around 130 papers, and we have conducted the 3 stage paper review process including abstract, full paper, and onsite oral presentation. Thanks to the IMPACT Technical Program Committees, paper reviewers, and session chairs' great support, we are delighted to announce those papers that have been selected for the IMPACT 2023 Paper Award.



Award Category	Paper Code	Paper Title	Author List	Affiliation
Packaging - Best Paper Award	TW0024	AI-based Adaptive Surrogate Modeling: A Future Performance Prediction Method Applied to UV-LED Modules	Cadmus Yuan	Feng Chia University
	AS0011	Modeling and Predicting the Beam Properties from Grating Structures using Deep Neural Network	Yu Dian Lim, Peng Zhao, Luca Guidoni, Jean-Pierre Likforman, Theo Henner, Chuan Seng Tan	Nanyang Technological University
	TW0030	Advanced Optical Metrology for Stability Monitoring of Polyimide Curing Process	Wen-Yi Lin, Kan-Ju Yang, Chia-Peng Sun, An-Dih Yu, Bei-Chun Huang, Kai-Cheng Chen, Yu-Sheng Wang, Cheng-Xuan Wu, Chien-Chen Li, Zhi-Hua Zou, Chien-Li Kuo	TSMC
Packaging - Best Student Award	AS0071	Fitting Anand Model Parameters with Artificial Neural Networks	Qinghua Su, K.N. Chiang	National Tsing Hua University
	TW0064	Use Artificial Neural Network to fit stress-strain curve of Chaboche model on lead-free solder SAC305	Cheng-En Lee, Cadmus Yuan, Kuo-Ning Chiang	National Tsing Hua University
	TW0079	Theoretical and Numerical Modeling of Thermal Warpages of DIMM Socket-Server PCB Assembly	YU WEN WANG	Chang Gung University
Packaging- Best Poster Award	TW0055	Fan-out Wafer-level Packaging Process Integration for Artificial Intelligence Real Dies	T. Y. Ouyang, O. Y. Xiovo, R. S. Cheng, Y. S. Chang, T. Y. Hung, C. K. Lee, and Y. M. Lin	ITRI
PCB-Best Paper Award	TW0099	Asymmetric Hybrid PCB Design for Cost-effective and Performance-driven Solution in Data Center Platforms	John Lin, Aje Chang, Alan Sun, Kaspar Tsang, Gause Hu, Jimmy Hsu, Brian Ho, Ryan Chang, Thomas Su	Intel
	EU0156	Revolutionizing The Bonding System for Ultra Fine-line Package Substrate Fabrication	Thomas Thomas, Christopher A. Seidemann, Thomas Huelsmann, Valentina Belova-Magri, Yuan Zou, Ken Kim, Patrick Brooks	MKS' Atotech
PCB-Best Student Award	AS0152	Electrical Conductivity Control of Stretchable Printed Wires for In-mold Electronics Applications	Reina Oshima	Gunma University
	TW0145	Improving the Uniformity of Electroplated Cu in Through Glass Via (TGV)	Yu-Ming Lin, Pei-Yu Yeh, Cheng-Yu Lee, Kuan-Hsueh Lin, Cheng-Chi Wang, and Cheng-En Ho	Yuan Ze University
PCB-Best Poster Award	EU0126	X-ray Photoelectron Spectroscopy (XPS) Investigations to Monitor the Cleanliness of Copper Surfaces during Palladium-Free Colloidal Copper Activation	Ibbi Y. Ahmet*, Andre Beyer, Laurence J. Gregoriades, Julia Lehmann, Yvonne Welz	MKS' Atotech



Hotel Information

To enjoy the discount for IMPACT conference attendees, please book your hotel right away and make further follow-up confirmations with the hotel.

Hotel	Information
The Evergreen Laurel Hotel Taipei 台北長榮桂冠酒店 Tel: +886-2-2501-9988	Taiwan Taoyuan International Airport—35mins by airport shuttle bus Taipei Songshan Airport—15mins by taxi MRT—5 mins by walk (Songjiang nanjing) *Near Xingtian Temple
The Place Taipei 南港老爺行旅 Tel: +886-2-7750-0588	Taiwan Taoyuan International Airport—45mins by taxi Taipei Songshan Airport—20 mins by taxi MRT —5 mins by walk (Gangang Software Park) *Near Nangang Exhibition Center
Caesar Park 台北凱撒大飯店 Tel: +886-2-2311-5151	Taiwan Taoyuan International Airport—40 mins by Taoyuan Airport MRT Taipei Songshan Airport—15 mins by taxi MRT —3 mins by walk (Taipei Main) *Near Taipei Main Station
Grand Hyatt Taipei 台北君悅酒店 Tel:+886-2-2720-1234	Taiwan Taoyuan International Airport—45 mins by taxi Taipei Songshan Airport—15 mins by taxi MRT —5 mins by walk (Taipei 101/World Trade Center) *Near Taipei 101

Inquiries

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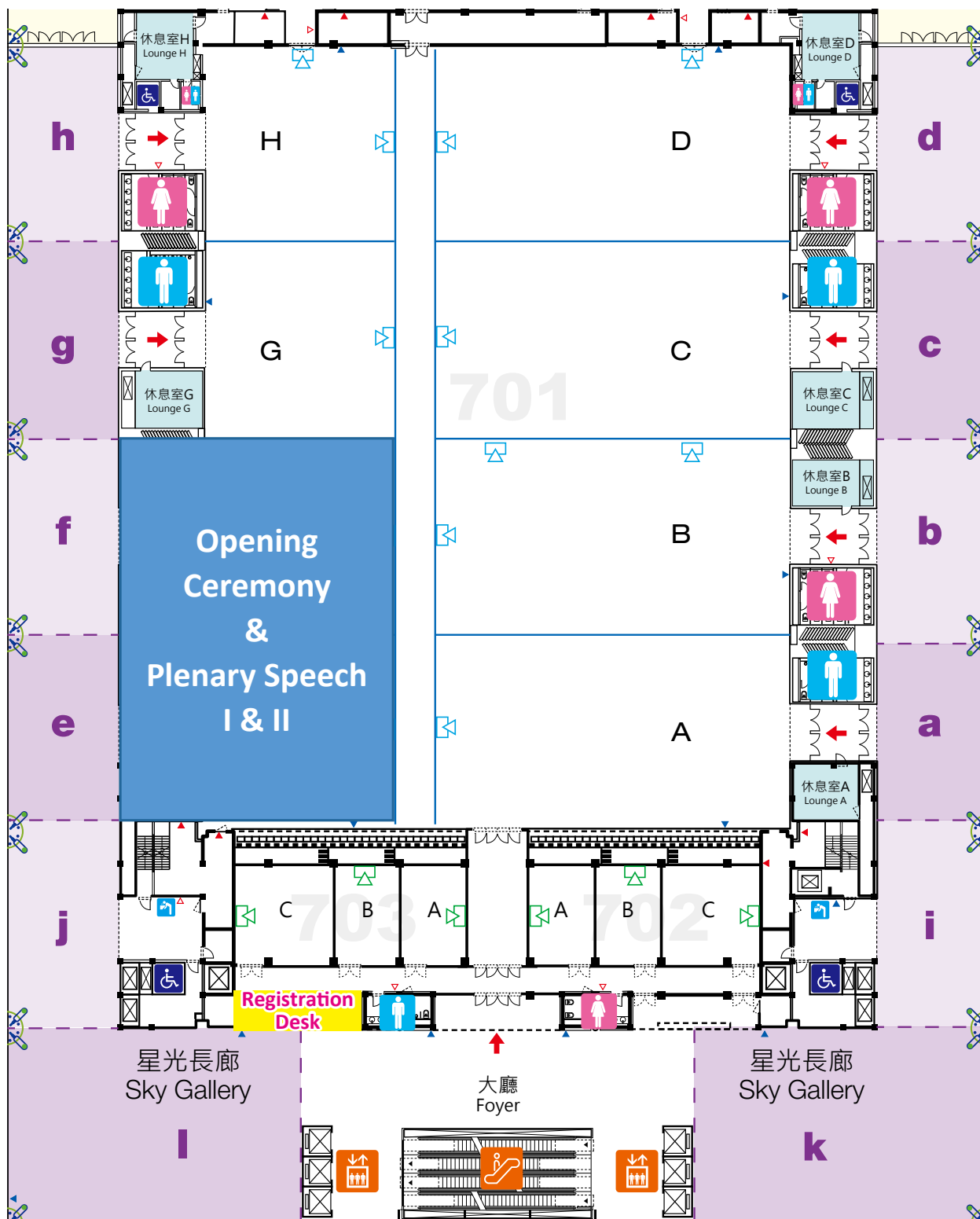


Opening Ceremony & Best Paper Awards Ceremony

Time: 10:00-10:20, Wednesday, October 23, 2024 (Registration starts from 9:00 am)

Location: 701EF, Taipei Nangang Exhibition Center, Hall 2

Chair: Shen-Li Fu, Ph.D, General Chair of IMPACT 2024



PLENARY SPEECH

Wednesday, Oct. 23th, 10:20-11:10



Hidehiro Tsukano

Senior Vice President
NTT

Topic: PEC Technology Evolution in IOWN for More than Moore

Room 701EF, TaiNEX 2

Outline

This presentation describes the features of PEC (Photonics-Electronics Convergence), which is promising in the pursuit of More than Moore along with ultra-fine semiconductor manufacturing processes and ultra-high density assembly, while covering the key points for chiplet design. IOWN (Innovative Optical and Wireless Network) initiative by NTT is a project to create a new information and communication processing infrastructure that overcomes traditional limits. It remarkably offers high-capacity, high-quality, low-latency, and low-power consumption, powered by advanced optical technology as its driving force. NTT has been conducting research and development according to a roadmap that aims to ultimately leverage the optical technology of communications, enabling optical wiring between computer boards, between packages, and within packages. This challenge endeavors to reduce the ever-increasing power consumption driven by advancements in AI worldwide. By further extending Moore's Law, PEC technology contributes to achieving carbon neutrality for a wide range of IT devices, from large-scale servers to user terminals.

Bio

Mr. Hidehiro Tsukano joined Fujitsu Limited in 1981, where he worked in the purchasing department, focusing on semiconductors. In his career at Fujitsu, he became head of Corporate Planning and Business Strategy Office in 2009 and representative director, senior executive vice president, and CFO in 2017. He has also served as chief strategy officer, in charge of all departments as assistant to the president. In 2019, he became vice chairman of the company.

After working as an advisor to NTT Advanced Technology Corporation in 2020 and senior advisor in the Research and Development Planning Department of NTT, he became the head of NTT IOWN Integrated Innovation Center in July 2021. He also serves as president & CEO, NTT Innovative Devices Corporation, which was established in August 2023.

Wednesday, Oct. 23th, 11:10-12:00**Dr. C.S. Yoo**

Vice President, Research & Development / More-than-Moore Technologies
Technologies at Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC)

Topic: Specialty Technology

Room 701EF, TaiNEX 2

Outline

While the leading- node technologies continue to push for ever smaller device geometries, faster speed, lower power and lower cost, Specialty Technology focus on adding special device features on a Si chip so as to enable various functionalities for different applications. To name a few, CMOS Image Sensor (CIS) adds a sensor (diodes) structure onto a Si chip; the HV has a device structure that can endure high voltage operations, and, the Embedded Memories, on the hand, build RRAM or MRAM structure in the backend of a Si chip processes. As called for by various applications, Specialty Technology proliferates over time. In this presentation, several Specialty Technology features and evolution will be introduced. Specialty Technology development can be very challenging, as it does, sometimes, need to leverage the leading-edge process and equipment to get the job well done. Specialty technology when orchestrated with the advanced nodes technology spring up countless applications that bridge the digital world to people.

Bio

After receiving his PhD from Chemical Engineering at WPI (Worcester Polytechnic Institute) in 1988, CS joined TSMC as a Technical Staff in RD, working on Photolithography and Thin Films. He evaluated the 1st ASML stepper into tsmc . Then, he took on various manager positions in Module development, SRAM and Embedded DRAM development. He led his team in developing a novel triple-poly SRAM structure that jacked up the gross dies per wafer by nearly 1.5 times.

He then spent more than 15 years in leading nodes' mask RD and EBO (e-beam Operation), where he and his team developed the 1st EUV pellicle for EUV production.

Following a two-year stint as the Program Manager for a major business account, he was back to RD for Specialty Technology Development in 2021. CS has over 60 patents and 30 publications, mostly in semiconductor technology. He enjoys playing tennis with someone he has no chance of winning; he is fond of reading something that he has difficulties in understanding.



Thursday, Oct. 24th, 9:00-9:50



Ki-III Moon

VP and Head of Packaging Development
SK hynix Inc.

**Topic: Advanced Packaging Technologies in Memory
Applications for AI Era**

Room 504, TaiNEX 1

Outline

Introducing the emerging PKG technology solutions for artificial intelligence.

I will review the development trends of PKG technology and define the core technologies needed in the future.

I will introduce PKG technology trends for high-bandwidth memory (HBM) and heterogeneous chips and explain SK hynix development direction.

Bio

Mr. Ki-III Moon is currently the Vice President of PKG Technology Development at SK hynix.

He graduated from Sogang University in 1996 and joined Hynix in the same year as a PKG product engineer, a position he held until 2011.

After 2011, he worked as a researcher at Hynix Japan Technology Center for four years.

From 2014 to 2017, he served as SK hynix Materials Development chief Manager, and since 2018, he has been in charge of SK hynix Technology Development .

He has more than 27 years of experience in the field, and his main areas of expertise are in advanced packaging, high-bandwidth memory (HBM), and heterogeneous integration.

Thursday, Oct. 24th, 9:50-10:40**Glenn Daves**

Senior Vice President of Package Innovation
NXP Semiconductors.

Topic: Heterogeneous Integration for Edge Applications

Room 504, TaiNEX 1

Outline

As the connected world continues to expand, the performance demands for these edge applications expand as well. From smart homes to smart farms and factories, to smart cars, edge computing applications are posing increasing challenges to product designers and to the packaging that enables them. These applications are housed far from the data centers in active environments, are highly power, thermal, and cost sensitive, and leverage diverse functions and semiconductor technologies.

Thus, they drive the need for new and differentiated packaging and heterogeneous integration technologies to support them. The keynote will explore these emerging market and technology dynamics, providing relevant examples.

Bio

Glenn G. Daves is Senior Vice President of Package Innovation at NXP Semiconductors. He is responsible for package design, package technology development, and assembly process development in support of NXP's full product portfolio. Prior to its acquisition by NXP, Glenn led packaging and printed circuit board development for Freescale Semiconductor. Prior to that, he led global packaging product and technology development at the IBM Corporation.

He has also held leadership positions in project management, test and burn-in engineering, and assembly manufacturing engineering. Glenn holds twenty- seven U.S. patents and has degrees from Brown University, the University of Illinois at Urbana-Champaign, and Alliance Theological Seminary. He serves on the National Leadership Council of World Vision U.S.



SESSION INTRODUCTION

ORAL PRESENTATION





SESSION 1: Ecosystem Enabling for Intel Data Center AI Server Solutions(Intel)

Time: 13:30-15:30, Oct 23, 2024

Chair: Jimmy Hsu, Intel

George Chen, Intel

Room: 504A

Time	Topic	Lead Author	Affiliation
13:30-14:00	System Architecture of Intel Data Center AI Server Solutions	 Gerry Juan	Intel
14:00-14:30	Cooling the Future: Navigating the Frontiers of Advanced Cooling Technologies	 Jay Wu	Intel
14:30-15:00	48V System Power Distribution: Design Challenge Analysis	 Kevin Liang	Intel
15:00-15:30	PCB Design Challenges and Electrical Characterization Evolution for High-speed Data Center AI Application	 Jimmy Hsu	Intel



SESSION 2: Evolution of Chiplet packaging architectures advancing AI and HPC growth(MKS' Atotech)

Time: 13:30-15:30, Oct 23, 2024

Room: 504B

Chair: Eddy Chen, MKS' Atotech


Time	Topic	Lead Author	Affiliation
13:30-14:00	Evolution of Chiplet packaging architectures advancing AI and HPC growth	 Daniel Ng	AMD
14:00-14:20	AI Driving a Transformative Era in Chiplet & Packaging Technologies	 Rozalia Beica	Rapidus
14:20-14:40	Ultra-High density RDL on Glass Core Substrate for Heterogenous Integration	 Satoru Kuramochi	Dai Nippon Printing Co., Ltd.
14:40-15:00	Advanced PCBs for AI chips	 Greg Link	WUS Printed Circuit
		 Sompol Chaloeicheep	WUS Printed Circuit
15:00-15:15	Advanced AI packages the transition form organic to glass core	 Kuldip Johal	MKS' Atotech
15:15-15:30	Process solutions for advanced PCBs supporting the needs for AI package manufacturing	 Frank Bruening	MKS' Atotech

SESSION 3: Advanced Packaging Technologies-1

Time: 13:30-15:30, Oct 23, 2024

Chair: Andrew Tay, National Singapore University
Ming-Yi Tsai, Chang Gung University

Room: 504C

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-14:00	Invited	Industrial Testing of 3D Heterogeneous Chip-Package-PCB-Antenna Modules via Advanced Electromagnetic-Thermal Analysis	 Andrew Tay	National University of Singapore
14:00-14:15	AS0145	Development of Polymer base Hybrid bonding Process	Masao Tomikawa	Toray Industries Inc.
14:15-14:30	AS0068	Cu-Cu Bonding at 200°C using a Copper Surface Treatment Solution that Activates the Copper Electrode Surface for Hybrid Bonding	Hirokatsu Sakamoto	Daicel Corporation
14:30-14:45	AS0052	Utilization of Au passivation nanolayer for low-temperature Cu-to-Cu bonding	Sangmin Lee	Seoul National University of Science and Technology
14:45-15:00	TW0104	Effects of a bi-layer of TFMG/Cu as a diffusion barrier in a Cu/Sn/Cu bonding structure for three-dimensional interconnects.	Chi-Hang Lin	National Chung Hsing University
15:00-15:15	TW0043	Fan-out Panel Level Packages Die Shift and Moisture-Thermal Coupled Stress Analyses	Sheng-Jye Hwang	National Cheng Kung University
15:15-15:30	TW0010	Advanced Optical Metrology Using on Surface Morphology Characterization of Polyimide for Process Quality Enhancement	Kan Ju Yang	Taiwan Semiconductor Manufacturing Company


SESSION 4: Design, Modeling, AI/Machine Learning Applications, and Testing -1

Time: 13:30-15:00, Oct 23, 2024

Room: 503

Chair: Dongkai Shangguan, Indium Corp.

Sheng-Jye Hwang, National Cheng Kung University

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-14:00	Invited	Thermal Test Vehicles for Characterization of Thermal Performance of AI Chips	 Dongkai Shangguan	IEEE Fellow, IMAPS Fellow
14:00-14:15	AS0118	Electrical Characterization and Testing of BGA Gripper-Type Socket for High-Speed Applications	Shadi Harb	Intel Corporation
14:15-14:30	AS0069	Enhancing Printed Circuit Board (PCB) Electrical Characteristics under Immersion Cooling Condition	Huafang Ju	Intel China Ltd.
14:30-14:45	AS0100	RSM Methodology for Accuracy Enhancement in SerDes Channel Solution Analysis	Wei Jern Tan	Advanced Micro Devices Global Services (Malaysia)
14:45-15:00	US0028	Predicting Wrinkle Formation in Flexible Thin-Film Structures	Yu-Lin Shen	University of New Mexico



SESSION 5: Sustainable Technologies & Systems

Time: 13:30-14:30, Oct 23, 2024

Chair: Alex King, Taimide Tech. Inc.

Kuo-Chan Chiou, ITRI

Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-13:45	US0146	Application of electrolytic membrane separation methods to achieve economical Zero Liquid Discharge Closed Loop Recycling in Printed Circuit Board and IC Substrate Manufacturing	Alexander Stepinski	Smart Process Design
13:45-14:00	US0090	Green Technology - Enabling Productivity and Sustainability for IC Substrate Manufacturing	Ryan Wagner	MKS Instruments
14:00-14:15	TW0120	A Novel Design of Compliant Mechanisms under Corrosive Environment	Fuhua Jen	Minghsin University of Science and Technology
14:15-14:30	EU0128	Innovative Approaches to Sustainable Manufacturing: Solvent-Free Copper Extraction and Zero Liquid Discharge Implementation	Gustavo Ramos	GreenSource Engineering






SESSION 6: Server Solution Customer SI+EV Enablement (AMD)

Time: 16:00-18:00, Oct 23, 2024

Chair: Hellen Lo, AMD

Yuan-Liang Li, AMD

Room: 504A

Time	Topic	Lead Author	Affiliation
16:00-16:24	A Reliable and Scalable nPI-based Statistical Methodology for Post-Silicon IO Testing and Validation Pre-recorded	 Anupriya Sriramulu	AMD
16:24-16:48	Cable Bending Impact to High-Speed SERDES	 Abdul Rais Abdul Rahim	AMD
16:48-17:12	PCIE Gen5 RX CEM RX Compliance Simulation Methodology	 Hellen Lo	AMD
17:12-17:36	System Board Passive Channel Validation with Impedance Correction De-embedded Method	 Yuan-Liang Li	AMD
17:36-18:00	Comparative Analysis of Signal Integrity and Cost Efficiency in high speed Serdes: Via-in-Pad vs. Non Via-in-Pad PCB Designs	 Cooper Li	AMD



SESSION 7: Topics for advanced packaging processes in Japan (JIEP)

Time: 16:00-18:00, Oct 23, 2024

Chair: Takeyasu Saito, Osaka Metropolitan University
Yuki Ishikawa, Sanyu rec Co.,Ltd

Room: 504B

Time	Topic	Lead Author	Affiliation
16:00-16:20	Development of Copper Plating Chemical for Through Silicon Via and Hybrid Bonding	 Reito Kobayashi	JCU corporation
16:20-16:40	Electrodeposition of Roughened Copper Plating by PR Pulsed Electrodeposition and Reliability Evaluation.	 Ryota Naka	OKUNO CHEMICAL INDUSTRIES Co.Ltd., Japan
16:40-17:00	Ultra-Compact VCSEL-based Optical Transceivers using 0.3-mm Pitch LGA Interface for Co-Packaged Optics	 Wataru Yoshida	Furukawa Electric Co., Ltd.
17:00-17:20	Evaluation of the bonding properties of die-bonded parts using formate-coated Sn-Zn solder sheets	 Koji YAMAZAKI	Gunma University
17:20-17:40	Development of polymer fine via etching technology for 3D chiplet integration	 Fumito Ootake	ULVAC, Inc.
17:40-18:00	Formation of 10 μm Pitch Sharp Micro-bump by Fusion Process of Imprint and Photolithography	 Kiyokazu Itoi	Panasonic Holdings Corporation


SESSION 8: Advanced Packaging Technologies-2

Time: 16:00-18:00, Oct 23, 2024

Chair: Andreas Ostmann, Fraunhofer IZM

Room: 504C

Shih-Kang Lin, National Cheng Kung University

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	High-Density Substrates for Chiplet Technology	 Andreas Ostmann	Fraunhofer IZM
16:30-16:45	AS0019	Elimination of Ti Residue Caused Yield Loss for Panel Level Package	Pradeep Sharma	NXP Semiconductors Limited
16:45-17:00	TW0087	Low Warpage Chip First FOPLP with Multi-Die and Fine Line RDL by Using Digital Lithography	Terry Wang	ITRI
17:00-17:15	AS0082	A Study of Efficiency of Total Volume of Mold Resin for Warpage in COW Process	Wataru Doi	Murata Manufacturing Co.,Ltd
17:15-17:30	TW0044	Precise Prediction of Capillary Underfill Process for Flip-Chip Packages	Sheng-Jye Hwang	National Cheng Kung University
17:30-17:45	AS0034	Optimizing the Effect of O2 Plasma on Cu Bonding for Cu Hybrid Bonding	Sangwoo Park	Seoul National University of Science and Technology
17:45-18:00	AS0074	Research on the Crystallinity of Metal Passivation Layer for Improving Low-Temperature Copper Bonding Performance	Min Seong Jeong	Seoul National University of Science and Technology




SESSION 9: HDI, IC Substrate and FPC Technology-1

Time: 16:00-18:00, Oct 23, 2024

Chair: Yu-Hua Chen, Unimicron

Room: 503

Nishimura Yoshio, Ajinomoto Co., Inc.

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	Advanced Insulating Material for Next-Generation Package	 Nishimura Yoshio	Ajinomoto Co., Inc.
16:30-16:45	EU0169	Mature Defect-Free Microprocessing for Advanced IC Substrates	Richard Noack	LPKF Laser & Electronics SE
16:45-17:00	US0091	New, Ultra-Low Loss Substrate Material offer Better Manufacturability	Jack Frankosky	The Chemours Company
17:00-17:15	EU0085	Electroless plating of ENEPIG and EPAG – comparing the impact of Pd-bath type and Au-bath type on the deposit properties and manufacturing conditions.	Britta Schafsteller	Atotech Deutschland GmbH
17:15-17:30	AS0031	Effect of Pulse-Reverse Electrodeposition Parameters on Throwing Power and Copper Thickness of the Microvia Pre-recorded	Rongbiao Shen	Delton Technology (Guang Zhou) INC.
17:30-17:45	US0157	Advanced Viafill Reliability Using Direct Metallization Technology	Carmichael Gugliotti	MacDermid Alpha
17:45-18:00	TW0070	Study of Solder Resist Undercut for Flip Chip Chip Scale Package Substrate	Ming Yu Chiang	SPIL


SESSION 10: Power Electronics Packaging-1

Time: 16:00-17:45, Oct 23, 2024

Chair: Li-Cheng Shen, USI






Chun-Kai Liu, ITRI

Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	USI's development of "VRM (Voltage Regulator Module) for HPC/AI applications"	 Li-Cheng Shen	USI
16:30-16:45	EU0089	In-situ condition monitoring of SiC-MOSFETs during active power cycling using acoustic emission testing	David Strahringer	Universität Freiburg
16:45-17:00	TW0135	Design and Simulation of Double Pulse Tests for Si IGBT/SiC MOSFET Hybrid Switch Power Module Applied to Electric Vehicles	Shu-You Lian	National Tsing Hua University
17:00-17:15	TW0155	Power Efficiency Characterization of Bidirectional Bridgeless Interleaved Totem-Pole PFC Boost Converter Using SiC-based Power Module	Wen You Jhu	Feng Chia University
17:15-17:30	EU0177	3D Stress Mapping in Processed SiC Wafers by Hyperspectral Raman Spectroscopy	Anton Myalitsin	ANVOS Analytics Co., Ltd.
17:30-17:45	TW0046	First 3.3kV/400A All-SiC Power Module Assembled in Taiwan: Outstanding Performance in Inductance, Thermal Resistance, and Switching Loss	I-Hung Chiang	ITRI



SESSION 11: IEEE EPS Panel, Heterogeneous Integration Roadmap (HIR) Compact Session
Time: 10:40-12:10, Oct 24, 2024 Room: 504
Chair: CP Hung, ASE

Time	Topic	Lead Author	Affiliation
10:40-10:45	Opening Remark	 CP Hung	ASE
10:45-10:55	Microsystem Integration for AI/Compute and Interface	 Chih-Ming Hung	Mediatek
10:55-11:05	Interconnect hierarchy in HI systems	 Chris Scanlan	IMAPS
11:05-11:15	HIR Brief	 William Chen	IEEE-EPS
11:15-12:10	Panel Discussion Panelist: Glenn Daves, SVP, NXP CM Hung, AVP, Mediatek Chris Scanlan, Director, IMAPS/SVP, Besi William Chen, HIR Chair, IEEE-EPS/Fellow, ASE	 Moderator :CP Hung	ASE





SESSION 12: Shaping Our Future with AI by Next-Gen Substrate and Packaging(DUPONT)

Time: 13:30-15:30, Oct 24, 2024

Chair: Lucy Wei, DUPONT

Room: 504A

Jason Chuang, DUPONT

Time	Topic	Lead Author	Affiliation
13:30-14:00	Organic Substrate Characteristics: Addressing Advanced Packaging Interconnect Challenges	 Ami Eitan	Taiwan Semiconductor Manufacturing Company
14:00-14:30	Convergence and Evolution of Advanced Package Materials	 Ki Seok Kim	Samsung Electronics
14:30-15:00	The Challenges and Opportunities of IC Substrates in The Age of AI	 Yiho Chen	Leading Interconnect Semiconductor Technology
15:00-15:15	Revolutionizing Advanced Packaging with Next-Gen Bump Plating Technology	 Renay Su	DuPont Interconnect Solutions
15:15-15:30	The Future is Now: Novel Seed Layer Formation on Glass Substrates with Mild Process Conditions for Advanced Packaging	 Vincent Hsu	DuPont Interconnect Solutions








SESSION 13: Market trend-Innovative 3D IC Heterogeneous Integration Packaging

Time: 13:30-15:30, Oct 24, 2024

Room: 504B

Chair: Albert Lan, Applied Materials

Time	Topic	Lead Author	Affiliation
13:30-13:54	Strategic Crossroads: Taiwan's Semiconductor Industry Amid US-China Geopolitical Tensions	 Rocky L. Uriankhai	SciTech Power Research Ltd.
13:54-14:18	The Future Display and Packaging Technology for Augmented Reality (AR)	 Yung-Yu Hsu	Meta
14:18-14:42	The Trend of Circular Economy and Application in E&E Industry	 Stephen Pao	SGS
14:42-15:06	Innovative Heterogeneous Integration Process and Tool Packaging Solutions Applying in AI/ HPC	 Albert Lan	Applied Materials
15:06-15:30	Navigating the Advanced packaging Industry: 2024 Market and Technology Trends	 Bilal HACHEMI	Yole Group

TPCA






SESSION 14: ICEP

Time: 13:30-15:30, Oct 23, 2024

Chair: Yasumitsu Orie, Rapidus

Yasuhiro Morikawa, ULVAC Inc.

Room: 504C


Time	Topic	Lead Author	Affiliation
13:30-13:54	Physical and Thermal Characteristics of the Advanced Package with Glass Core Substrate	 Shun Mitarai	Sony Semiconductor Solutions Corporation
13:54-14:18	Ideal Copper Wiring Formation by Silver-seed Semi-Additive Process for Semiconductor Package Substrates	 Wataru Fujikawa	DIC Corporation
14:18-14:42	Improvement of the Bonding Reliability of Electroless Thin-film Ni/Au Plating Using Co Activation	 Kana Kawasaki	Okuno Chemical Industries Co., Ltd.
14:42-15:06	NGK Ceramic Products for Semiconductor Modules	 Masashi Kuwabara	NGK Insulators, Ltd.
15:06-15:30	Semiconductor Package Substrate Trend and Requirement for Advanced Package	 Kiyoshi Oi	SHINKO ELECTRIC INDUSTRIES CO., LTD.

SESSION 15: Advanced Packaging Technologies-3

Time: 13:30-15:30, Oct 24, 2024

Chair: Po-Hao Tsai, Applied Materials
Haley Fu, iNEMI

Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-14:00	Invited	Advancing Packaging Technology: Exploring Through Glass Vias for Glass Core Integration as an Alternative to Si Interposer	 Herbert Oetzlinger	Lam Research
14:00-14:15	TW0050	Homogeneous Integration Fan-out Chip Module Warpage Control Solutions	Feng Kao	SPIL
14:15-14:30	TW0040	Optimal High Speed Signal Design for Universal Chiplet Interconnect Express (UCIe) Application	Hsu Terry	SPIL
14:30-14:45	EU0185	Direct wet chemical copper metallization process on glass substrates	Thomas Thomas	Atotech Deutschland GmbH
14:45-15:00	TW0187	Applying Hybrid Numerical Simulation of Capillary Underfill Flow to Advanced Packaging Technologies in Fine Pitch Multi-Chip Modules	Chien-Ting Wu	Moldex3D
15:00-15:15	TW0162	Estimating Warpage of Fan-Out Panel-Level Packages under Different Manufacturing Processes Using a Viscoplastic Model	Ming Ching Huang	National Tsing Hua University
15:15-15:30	TW0179	Investigation of bonding between nanotwinned Cu and nanocrystalline Cu	Po-Hung Lai	National Yang Ming Chiao Tung University


SESSION 16: Design, Modeling, AI/Machine Learning Applications, and Testing -2

Time: 13:30-15:30, Oct 24, 2024

Chair: Meng-Kai Shih, National Sun Yat-sen University

Room: 502

Shu-Shen Yeh, Google

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-14:00	Invited	Surface activated bonding as promising wafer process technologies for creating novel advanced devices	 Naoteru Shigekawa	Osaka Metropolitan University
14:00-14:15	TW0065	Variable Switching Frequency Global Driving Strategy of SiC-MOSFET and Si-IGBT-based Motor Drive System for Electric Vehicle Applications	Yow Luen Lim	ITRI
14:15-14:30	TW0059	Warpage Optimization Design for FOPOP by Using Finite Element Analysis and Statistical Analysis	Ken Zhang	SPII
14:30-14:45	TW0103	A fracture mechanics model for interface debonding in 2.5-d package under solder reflow	Tz-Cheng Chiu	National Cheng Kung University
14:45-15:00	TW0053	Co-Design Optimization for PI SI When Considering Thermal Performance	Peater Wu	Amkor Advanced Technology
15:00-15:15	TW0020	Characterization of Wafer Probing Needle and Optimization Design of Multi-layer Cantilever Probe Card Geometry	Mengkai Shih	National Formosa University
15:15-15:30	TW0112	Reliability Analysis of The Side-fill Reinforcement Technology Applied to Electronic Packaging by Finite Element Method	Chang-Chun Lee	National Tsing Hua University



SESSION 17: Advanced Packaging(SPIL)

Time: 16:00-18:00, Oct 24, 2024

Chair: Yu-Po Wang, SPIL

Kuo-Ming Chen, UMC

Room: 504A

Time	Topic	Lead Author	Affiliation
16:00-16:24	How to Characterize Bending Strength of Thin Dies	 Ming-Yi Tsai	Chang Gung University
16:24-16:48	PLP Advanced Packaging Global Overview	 Eu Poh Leng	NXP
16:48-17:12	IC Substrate Development Trend and Future Holds	 Carl Chen	SPIL
17:12-17:36	How InnoLux can groundbreaking the FOPLP application in advanced IC package	 George Lin	InnoLux Corporation
17:36-18:00	RDL Embedded Coreless Substrate for heterogeneous integration	 Fusao Takagi	Toppan





SPIL

SESSION 18: SMTA

Time: 16:00-18:00, Oct 24, 2024

Room: 504B

Chair: Jeffrey Lee, Integrated Service Technology Inc.

Time	Topic	Lead Author	Affiliation
16:00-16:30	Challenges of soldering in High Reliability Automotive Electronics	 NingCheng Lee	ShinePure High-Tech Corporation
16:30-17:00	Back to the Future - Integration the Features of BGA and QFN	 Charles Lin	Bridge Semiconductor
17:00-17:30	Innovative Interconnect Material for Advanced Packaging Assembly Process	 Lim Sze Pei	Indium Corp.
17:30-18:00	Reworkable edgeond enhances the reliability of large BGA assembly for board-level applications	 Simon Chang	Zymet Corp.



SESSION 19: Design, Modeling, AI/Machine Learning Applications, and Testing -2

Time: 16:00-17:30, Oct 24, 2024

Chair: Chun-Kai Liu, ITRI

Room: 504C

Chang-Chun Lee, National Tsing Hua University

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	Novel Quantum-Dot Color Conversion Film Fabrication for Mini-LED Applications	 Ricky Shi-Wei Lee	Hong Kong University of Science & Technology
16:30-16:45	AS0150	Design of Class AB Power Amplifier to Enhance Range of S-band Radar module using GaN HEMT	M Farhan Shahid	NUST
16:45-17:00	AS0139	Microstructural characterization of anisotropic evolution of sinter structure under high-temperature storage	Tomoki Matsuda	Osaka University
17:00-17:15	AS0134	Low Temperature Ag Sintering and Post Mold Cure Condition Effect on the Different Surface Finish Substrate using Ag Nano-porous Sheets	YehRi Kim	Korea institute of industrial technology
17:15-17:30	TW0114	System Level Heat Sink Design of Power Module for EV Application	Chun-Kai Liu	Industrial Technology Research Institute


SESSION 20: Advanced and Green Materials and Process-1

Time: 16:00-17:45, Oct 24, 2024

Chair: Jason Lee, Boardtek Electronics

Carl E. Chiang, TPCA

Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	Next-Generation 1.6T Switch & AI Server Materials and Design Trends	 Chieh-Sen Lee	Elite Material Co., Ltd
16:30-16:45	AS0012	Reduction of Permanganate Treatment Time in Wet Desmearing Process Using Vacuum Ultraviolet Irradiation from Excimer Lamp	Akihiro Shimizu	Ushio Inc.
16:45-17:00	TW0164	Comparative Study between Single and Array Antenna Characteristics with Different Surface Finishes	Yu Hsun Chang	Yuan Ze University
17:00-17:15	TW0094	Impact of Half-ounce Copper Foil Impact on PCB Electrical Characteristics in High-Layer Count Designs for High-Speed Data Center AI Systems	Ryan Chang	Intel
17:15-17:30	TW0072	Optimizing PCB Design with Advanced Copper Foil and Superior Oxide Treatment	Ann Yen	Intel
17:30-17:45	AS0136	Impact of Electrical Current Stressing on η^1 -Cu ₆ Sn ₅ in Electronics Packaging	Shubhayan Mukherjee	National Cheng Kung University



SESSION 21: Test, Quality, Inspection and Reliability / Simulation

Time: 16:00-17:45, Oct 24, 2024

Chair: Ben-Je Lwo, National Defense University

De-Shin Liu, National Chung Cheng University

Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
16:00-16:30	Invited	Optimizing Blind Microvia Manufacture to Enable Best in Class Reliability Performance	 Roger Massey	MKS Instruments Inc.
16:30-16:45	AS0039	Application of Sampling Moiré Method for Evaluating Residual Stresses in Resin-Molded Electronic Packages	Masaaki Koganemaru	Kagoshima University
16:45-17:00	US0027	The Impact of Recent Revision of ENEPIG Specification - IPC 4556A	Frank Xu	MacDermid Alpha Electronics Solutions
17:00-17:15	TW0165	Multi-Camera System with Advanced Image Correction Techniques for PCB Industrial Applications	Chao-Ching Ho	National Taipei University of Technology
17:15-17:30	TW0101	Impedance Matching Designs and Measurements of End-Launched Connectors Used in Multilayer Printed Circuit Boards	Chien-Chang Huang	Yuan Ze University
17:30-17:45	AS0021	The Via Impedance Simulation and Control in PCB Manufacture for 112Gb/s	Paul li	Delton technology inc
Pre-recorded				





SESSION 22: ISMP

Time: 08:20-10:20, Oct 25, 2024

Chair: Taek-Soo Kim, KAIST

Woosung Park, Hanyang University

Room: 504A





Time	Topic	Lead Author	Affiliation
08:20-08:44	Reliability Challenges in Advanced Packaging	 Young-Chang Joo	Seoul National Univeristy
08:44-09:08	Mechanical Reliability of Thin Film Materials for Semiconductors, Displays and More	 Taek-Soo Kim	KAIST
09:08-09:32	A study on the measurement of warpage and microstructures in advanced packaging and HBM manufacturing processes	 Joonho You	nexensor Inc.
09:32-09:56	Automatic prediction of thermal-mechanical properties of packaging substrate pattern design based on machine learning	 Eun-Ho Lee	Sungkyunkwan Univeristy
09:56-10:20	Multiscale thermal challenges in heterogeneous interfaces	 Woosung Park	Hanyang University

SESSION 23: Glass Substrate

Time: 08:20-10:20, Oct 25, 2024

Room: 504B

Chair: ONISHI Tetsuya, Grand Joint Technology


Time	Topic	Lead Author	Affiliation
08:20-08:50	The Role of Glass in Next Generation Substrate Technology: Opportunities and Challenges	 E. Jan Vardaman	TechSearch
08:50-09:20	Supporting the electronic packaging industry with glass substrates and structured glass substrate for the heterogeneous integration of electronic components.	 Martin Letz	SCHOTT AG
09:20-09:50	Panel Based Large Scale Glass substrate for High performance computing application	 Satoru Kuramochi	Dai Nippon Printing Co., Ltd.
09:50-10:20	Glass Package Technology Trends and Core Technologies	 ONISHI Tetsuya	Grand Joint Technology

SESSION 24: Interconnections & Nanotechnology

Time: 08:20-10:20, Oct 25, 2024

Chair: Takayuki Ohba, Institute of Science Tokyo
Chien-Lung Liang, NTUST

Room: 504C

Time	Paper Code	Topic	Lead Author	Affiliation
08:20-08:50	Invited	Anomaly factor clustering technology for high-speed transmission lines	 Yutaka Uematsu	Hitachi Ltd.
08:50-09:05	AS0064	TSV formation by direct Cu electroplating on electroless Co alloy barrier layer	Shoso Shingubara	Kansai University
09:05-09:20	TW0186	3D X-ray CT Study of Void Migration in Cu-filled Microvias under Electron Current Stressing	Cheng-En Ho	Yuan Ze University
09:20-09:35	TW0153	Microstructure Evolution and Electrical Resistance Transition in Micro Joints under Electron Current Stressing	Pei-Chia Hsu	Yuan Ze University
09:35-09:50	TW0127	Electromigration Failure Study of Advanced Flip-chip QFN Solder Interconnects with Various Metallization Combinations for High-power Automobile Applications	Chien-Lung Liang	National Taiwan University of Science and Technology
09:50-10:05	TW0113	Co-electrodeposition of nanotwinned copper-carbon nanotubes composite films with high mechanical properties	Ciao-Yun Luo	National Yang Ming Chiao Tung University
10:05-10:20	TW0092	Gallium Transient Liquid Phase Bonding for Cu-to-Cu interconnection	Tzu-Hsuan Huang	National Cheng Kung University




SESSION 25: HDI, IC Substrate and FPC Technology-2

Time: 08:20-10:05, Oct 25, 2024

Chair: Dyi-Chung Hu, Siplus

Michael Chang, Dupont

Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
08:20-08:50	Invited	Sustainable Technology for High-performance Computing	 Dyi-Chung Hu	Siplus
08:50-09:05	TW0009	Advanced Development of Embedded Technology on Ceramic Embedded Laminate (CEL) Structure for Thermal Applications	Liao Yu-Hsien	Tong Hsing Electronic Industry, LTD.
09:05-09:20	TW0023	Recent Advance of Low Silver Substrate for High Reliability Power Applications	Chih Wei Mao	Tong Hsing Electronic Industry, LTD.
09:20-09:35	TW0057	Advancements in Electroless Copper Plating for Via Shrinking Technology Trend	Vincent Hsu	DUPONT
09:35-09:50	TW0152 ☆	Effects of Substrate Roughness on Electroplated Cu Crystallographic Microstructure and Pinhole Formation	Pei-Chia Hsu	Yuan Ze University
09:50-10:05	TW0095 ☆	Optimization of High Aspect Ratio Through Glass Vias Void-Free Filling Using Complex System Response Platform	Yu-Ting Fu	National Tsing Hua University

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SESSION 26: Advanced Materials, Automatic Process & Assembly

Time: 08:20-10:35, Oct 25, 2024

Chair: Ting-Li Yang, Mediatek

Fan-Yi Ouyang, NTHU

Room: 502

Time	Paper Code	Topic	Lead Author	Affiliation
08:20-08:50	Invited	Latest 3D Analysis Technologies for semiconductor	 Hideki Hashimoto	Toray Research Center, Inc.
08:50-09:05	AS0154	Controlling Silver Micro-Fillers Sintering Behavior by Binder Chemistry for Enhancing Connection Properties of Epoxy-Based Conductive Adhesives	Takanori Fukushima	Gunma university
09:05-09:20	AS0035	Enhancement of electro-migration reliability by CCSB (Cu core solder ball) for solder interconnection material	Jaeyeol Son	MKE company / Sungkyunkwan university
09:20-09:35	EU0181	Pioneering the leading-edge adhesion enhancement system for the future of package substrates bonding	Thomas Thomas	Atotech Deutschland GmbH
09:35-09:50	AS0178	Controlling Interfacial Electrical Conductivity of Copper-filled Conductive Pastes for Improving Their Electrical Reliability	Masahiro Inoue	Gunma University
09:50-10:05	EU0042	Waving Warpage goodbye: UV for Fan-Out	Markus Schindler	DELO Industrial Adhesives
10:05-10:20	AS0029	Low temperature sintered copper nano/fine particles as joining materials	Tetsu Yonezawa	Hokkaido University
10:20-10:35	TW0066	A cost effective and eco-friendly solution for SiP package miniaturization and solder joint reinforcement	Kuo-Hua Hsieh	Wistron NeWeb Corporation



SESSION 27: Heterogeneous Integration

Time: 10:30-13:00, Oct 25, 2024

Chair: Shin-Puu Jeng, TSMC

Kathy Yan, TSMC

Room: 504A

Time	Topic	Lead Author	Affiliation
10:30-11:00	HPC Package Options to Address Pitch Scaling	 E. Jan Vardaman	TechSearch
11:00-11:30	Towards Sustainable AI/ML Clusters & Hyperscale Datacenters: The Advantages of RDL based 2.5D Interposers in High Bandwidth Routers and Switches	 Reza Sharifi	Broadcom
11:30-12:00	From Electrical and Testing Requirements to Foresee HPC Advanced Packaging Technology Development	 Chupei-Tang Wang	TSMC
12:00-12:30	Signal and Power Integrity Design of HBM3E-9.2Gbps for 2.5D-IC Heterogeneous Integration on Advanced Packaging Technology	 Sheng-Fan Yang	Global Unichip Corporation
12:30-13:00	Next Generation HBM and the Potential Impact of new strategies on sustainability	 Bret K Street	Micron Technology


SESSION 28: Advanced Packaging Technologies-4

Time: 10:30-12:30, Oct 25, 2024

Chair: Lih-Shan Chen, I-Shou University

Room: 504B

Myongchun Koh, Taiyo Ink MFG. Co., Ltd

Time	Paper Code	Topic	Lead Author	Affiliation
10:30-11:00	Invited	Novel photo imageable film for RDL of advanced package	 Myongchun Koh	Taiyo Ink MFG. Co., Ltd
11:00-11:15	TW0071	Signal Integrity Analysis of UCle Channel in FOCoS Advanced Package	Chiung-Ying Kuo	ASE Group
11:15-11:30	EU0037	Driving Efficiency and Reliability in Al Hardware: Leading Edge Pulse Plating Solutions for Uniform Copper Deposition	Mustafa Özkök	Atotech Deutschland GmbH
11:30-11:45	US0003	Advanced Electroplating Processes for IC Substrates – Redistribution Layer and Embedded Trenches	Saminda Dharmarathna	Macdermid Alpha Electronic Solutions
11:45-12:00	TW0129	Investigation of different wet pretreatment solutions for SiCN-SiCN bonding without TCB process	Chien-Yu Liu	National Yang Ming Chiao Tung University
12:00-12:15	TW0176	Surface modification for PI-to-PI direct bonding for advanced electronic packaging	Hsu Chih-Wei	National Chung Hsing University
12:15-12:30	TW0110	Integrated Delta-Sigma Modulator with Low Pass Filter for Acoustical Applications	Wen-Cheng Lai	National Yunlin University of Science and Technology




SESSION 29: Design, Modeling, AI/Machine Learning Applications, and Testing / Smart manufacturing

Time: 10:30-12:15, Oct 25, 2024

Chair: Yu-Jung Huang, I-Shou University

Room: 504C

Rozalia Beica, Rapidus

Time	Paper Code	Topic	Lead Author	Affiliation
10:30-11:00	Invited	Empowering Innovation: The Role of Advanced Interconnects in AI and Heterogeneous Integration	 Rozalia Beica	Rapidus
11:00-11:15	TW0171	Utilizing both Backplane and Cable Connections in Server Systems: Viability and Challenges in a Common AI Server Design	Thonas Su	Intel
11:15-11:30	TW0062	The Evaluation of Thermal Performance on Fan Out POP Package	Michael Fu	SPIL
11:30-11:45	TW0025	Bubbling Matters?	Dirack Lai	Wiwynn Corporation
11:45-12:00	TW0076	AI and AI-assisted Design for Reliability Approaches for Advanced Electronic Packaging: Review and Perspectives	Cadmus Yuan	Feng Chia University
12:00-12:15	US0156	Productivity Enhancement in Semiconductor Manufacturing with AI-enabled Operations Digital Twin Platform	Kaipei Yang	Plato Systems

SESSION 30: Advanced and Green Materials and Process-2

Time: 10:30-12:00, Oct 25, 2024

Chair: Chien-Lung Liang, NTUST

Simon Kuo, Cymmetrik

Room: 503

Time	Paper Code	Topic	Lead Author	Affiliation
10:30-10:45	TW0011	Advanced Lithography Solutions To Address Extreme Die Shifts in Fan-Out Panel-Level Packaging	John Chang	Rodulph
10:45-11:00	AS0079	Influence of Exposure Machine on the Reliability of White Solder Mask Layer on Printed Circuit Board	Hengxi Pan	Delton Technology (Guang Zhou) INC.
11:00-11:15	TW0144	Innovative Approaches to Streamline Manufacturing in Flexible Hybrid Printed Electronics (FHPE)	Shan-Jen (Simon) KUO	Cymmetrik
11:15-11:30	TW0117	Development of a Novel Solder Alloy for High Reliability Electronic Devices	Albert T. Wu	National Central University
11:30-11:45	TW0175	Development of hybrid surface treatment for SiO ₂ /SiO ₂ low temperature bonding in 3D IC packaging	Wei Zheng Li	National Chung Hsing University
11:45-12:00	TW0168	Plasma Descum on Advanced Packaging Development	Peng Yang	ASE Group




SESSION 31: Test, Quality, Inspection and Reliability / Smart Manufacturing

Time: 10:30-12:30, Oct 25, 2024

Room: 502

Chair: Jimmy Hsu, Intel Corporation

Kuan-Jung Chung, National Changhua University of Education

Time	Paper Code	Topic	Lead Author	Affiliation
10:30-11:00	invited	Transforming PCB Design and Electrical Characterization: Intel® Automatic In-Board Solution for Cutting-Edge Data Center and AI Application	 Jimmy Hsu	Intel Corporation
11:00-11:15	TW0077	Electrical Characterization and Analysis of High-Speed Data Center Platforms Utilizing Diverse De-embedding Methodologies	Tina Yang	Intel
11:15-11:30	TW0173 ☆	Inspection, Estimation, and Design of Hybrid Bonding in 3D IC Fabrication Using In-situ Heating Atomic Force Microscopy	Huai-En Lin	National Yang Ming Chiao Tung University
11:30-11:45	TW0047	Fracture Analysis of Micro-vias with Low to High Void Existence at Electroless Cu Plated Layers after Thermal Shock Reliability Cycle Test	Ming-chun Hsieh	Osaka University
11:45-12:00	TW0060	Experimental and Numerical Investigation on Dynamic Response of Flip Chip Package under Board Level Drop Test	ChiWei Wang	National Chung Cheng University
12:00-12:15	TW0122	Study on the Different Microstructures of Copper-to-Copper Joints on Electromigration Lifetime	Hsin Yu Tsai	National Yang Ming Chiao Tung University
12:15-12:30	TW0163	Investigating Human Mental Workload during Human Robot Interaction	Sheng-Yuan Chen	National Yang Ming Chiao Tung University

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SESSION 32: 3D embedding technology toward heterogeneous integration

Time: 13:30-15:30, Oct 25, 2024

Chair: Wei-Ta Yang, ITRI

Room: 504A

Yoshihisa Katoh, FUKUOKA-University

Time	Topic	Lead Author	Affiliation
13:30-14:00	Thermal and Mechanical Characterization Analysis of 2.5D IC and Advanced Fan-Out Packaging	 Meng-Kai Shih	National Sun Yat-sen University
14:00-14:30	System Level Co-Design Platform for 3D SiP & 3D electronic module	 Masaomi Suzuki	Zuken Inc.
14:30-15:00	Approaches to Next Generation Semiconductor Heterogeneous Integrated Packages	 Jun Mizuno	National Cheng Kung University
15:00-15:30	3D device embedded technology in IEC international standardization	 Yoshihisa Katoh	FUKUOKA-University

SESSION 33: Design, Modeling, AI/Machine Learning Applications, and Testing /Advanced Process

Time: 13:30-15:30, Oct 25, 2024

**Chair: Tz-Cheng Chiu, National Cheng Kung University
Lewis Huang, Senju Electronic (Taiwan) Co.,Ltd**

Room: 504B

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-13:45	AS0051	Novel Photo Imageable Film for RDL Application	Meiten Koh	Taiyo Ink MFG. Co. Ltd.,
13:45-14:00	AS0084	Multi-stepped Solder Resist Patterning Technology for Advanced IC Packaging	Yuya Suzuki	Taiyo America Inc.
14:00-14:15	TW0167	Using Uncertainty Analysis to Validate Reliability Prediction in WLP with Idealized Solder Joint Modeling	Yu-Ting Su	National Tsing Hua University
14:15-14:30	TW0106	3D PSF Deconvolution to Enhance Optical Critical Dimension Measurement and Extend Effective Depth-of-Focus in Microscopy	Yu-Tang Huang	National Taiwan University
14:30-14:45	TW0158	Determination of Biaxial Bending Strength of Thin Silicon Die in the Ball-on-Ring Test by Considering Contact Nonlinearity	Po Jen Hsieh	Chang Gung University
14:45-15:00	TW0166	Developing Pad Design Criteria for Wafer-Level Chip-Scale Package Through Pad Size Effect Analysis	Chih-An Yang	National Tsing Hua University
15:00-15:15	TW0015	Machine learning models with synthetic minority oversampling in predicting substrate warpage	Wan-Lu Hsu	National Chi Nan University
15:15-15:30	TW0174	Effects of light exposure pre-treatment on copper-to-copper direct bonding for advanced electronic packaging	Chun-Kai Lin	National Chung Hsing University

SESSION 34: Interconnections & Nanotechnology & Advanced Materials, Automatic Process & Assembly

Time: 13:30-15:15, Oct 25, 2024

Chair: Chih Hang Tung, TSMC

Room: 504C

Cheng-En Ho, Yuan Ze University

Time	Paper Code	Topic	Lead Author	Affiliation
13:30-13:45	AS0132	Flux-Less Solder Ball Attachment Technology (FLAT) for Advanced BGA Assembly	Dongjin Kim	Korea Institute of Industrial Technology (KITECH)
13:45-14:00	TW0140	Dimensional Effects on Grain Size and Surface Orientation of Nanocrystalline Cu in SiO ₂ Micro-vias	Te Hao Chao	National Yang Ming Chiao Tung University
14:00-14:15	TW0172	Effects of light exposure pre-treatment on Al-to-Al ultrasonic bonding	Ting Hsiang Hsueh	National Chung Hsing University
14:15-14:30	TW0170	The Improvement of Cu/PI Hybrid Bonding by Low-Wave Length Ultraviolet Light Pretreatment	Wei-Chien Tang	National Chung Hsing University
14:30-14:45	TW0151	Effect of plating temperature on the crystallization and texture development of highly (111) oriented electroless Cu nanotwins	Po Shao Shih	National Taiwan University
14:45-15:00	TW0124	Optimizing Cu-Cu Bonding Strength in Nanotwinned Cu Films Through Plasma-Induced Surface Roughening	Ming Chieh Chen	National Yang Ming Chiao Tung University
15:00-15:15	TW0119	A Study of a Plating Hanger for a Vertical Copper Electroplating Machinery	Fuhua Jen	Minghsin University of Science and Technology



Poster session I - Packaging

Time: 15:00-16:00, Oct 23, 2024

Chair: Hsiang-Chen Hsu, I-Shou University

Hung-Ying Tsai, National Tsing Hua University

Foyer Area

Paper Code	Topic	Lead Author	Affiliation
AS0024	Evaluation of Fly Cutting Planarization for Cu/polyimide Hybrid Bonding	Suin Jang	Seoul National University of Science and Technology
AS0032	Characterization of PVD SiCN dielectric for Hybrid Bonding Application	Jun Young Choi	Seoul National University of Science and Technology
AS0058	Study of Low Temperature Cu-to-Cu Bonding using Reducing Plasma Pretreatment	linda Li	Seoul National University of Science and Technology
AS0097	Analysis of Noise Coupling from 48V Voltage Regulator Common Module (VRCM) to High Speed I/O Traces	Shijuan Qin	Intel
AS0102	The Advanced DC Circuit Model for Hybrid bonding in Dual Damascene Structures	Seon Woo Kim	Seoul National University of Science and Technology
AS0105	Influence of Current Distribution Variations on Contact Resistance Measurement in Cu-Cu Bonding Interface	Kyoung Min Shin	Seoul National University of Science and Technology
AS0107	Optimizing Low-Temperature Polymer Thermo Compression Bonding and Polymer Patterning for 3D Multi-Chip Integration	Ji Hun Kim	Seoul National University of Science and Technology
AS0108	Characterization and Optimization of SiCN Films for Low-Temperature Cu Hybrid Bonding	Yeonju Kim	Seoul National University of Science and Technology
AS0121	Novel Advanced Packaging Materials: Low Dielectric Loss Siloxane Hybrids	Seung-Mo Kang	KAIST
AS0130	Interface characterization of fine pitch copper and polyimide L/S structures for improving RDL by AFM-IR and TEM-EELS technique	Hirofumi Seki	Toray Reserach Center, Inc.
AS0138	A Theoretical Study on the Global Analysis of New Multimodal Optical Metrology for Critical Dimension (CD) Measurement and Stress Analysis in Advanced Semiconductor Packaging	Surajit Das	National Taiwan University
TW0005	Advanced Solder Dispensing Process Evaluation for Miniaturization and 3D Assembly	Chih Yen Chen	USI, Universal Scientific Industrial

Paper Code	Topic	Lead Author	Affiliation
TW0013	Establish Deep Learning Model to Predict PCBA Reflow Profile	Kevin Hong	Universal Global Scientific Industrial Co., LTD
TW0017	Pre-fabricated Via Array Substrate for Programmable AIoT Applications	Tsung Yu Ou Yang	ITRI
TW0036	Fan-out RDL packaging process and shuttle service	Chenchun Yu	ITRI
TW0054	Optimization Via Impedance Feature Under High Density Fan-out Package Structure	Tsung Ting Lee	Amkor
TW0061	A novel polymer material for low-temperature hybrid bonding and flexible substrate applications	Yi-Hsuan Chen	National Yang Ming Chiao Tung University
TW0067	Impact of Manufacturing Techniques on Chip Strength: Flexural Testing and Weber Analysis	Yating Fan	PANJIT
TW0141	Ultra Thinning Wafer Structures with Controllable Backside Etch Stop Layer for HBM and BSPDN Applications	Yu-Chien Ko	National Yang Ming Chiao Tung university
TW0147	Molecule-based diffusion barrier layer for silicon/copper heterojunction	Tzu Yu Chu	National Chung Hsing University
TW0149	Warp Page Analysis of Thermo-Compression Bonding on The Coreless Substrate	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
TW0160	Warp Page and Stress Analysis in Molded 2.5D Package Chiplet Integration	Meng Chi Hsu	ASE



Poster session II - Packaging & PCB

Time: 15:00-16:00, Oct 24, 2024

Chair: Hsien-Chie Cheng, Feng Chia University

John Liu, TPCA

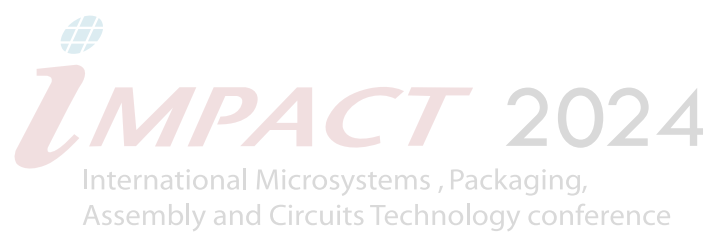
Foyer Area

Paper Code	Topic	Lead Author	Affiliation
AS0045	Enabling E-less NiPdAu top metal for clip and Cu/Au wire bonding in a hybrid Package	Linda Li	Nexperia
AS0048	Performance and Power Analysis on Immersion Cooling Solutions	Jasen Jing	Intel APAC R&D
AS0073	Reduced Fluorine Content of Fluorinated Polyimide / Fumed Silica Composites with Improved Tensile Properties	In Park	Korea Institute of Industrial Technology
AS0080	Development of high heat dissipation thermosetting sintering Cu paste	Yusuke Nuida	ADEKA Corporation
AS0081	Lowering temperature of Cu sinter-bonding in the air by controlling morphology of Cu particles with plasma spray physical vapor deposition	Miwa Oba	Osaka University
AS0098	Low-temperature Direct Ag Sinter Bonding to SiC Utilizing Ag Migration Assisted by Electric Field	Tetsuhiro Matsuda	Osaka University
AS0111	Improvement of mechanical joint property utilizing sintered structure with graded deformability	Takuya Okamoto	Osaka University
TW0002	TEM Analysis on Nano Defects of Chip Bonding Component Materials	Chi-Hang Tsai	Industrial Technology Research Institute (ITRI)
TW0004	Transmission Line Designs for 5G Fan Out Antenna in Packaging	Ben-Je Lwo	National Defense University
TW0026	A High performance Black PI EMI Shielding Film in Flexible Printed Circuit (FPC)	Yuang Chi Lee	Asia Electronic Material Co
TW0030	Positive dry film photoresist material	Ming Tzung Wu	Industrial Technology Research Institute(ITRI)/MCL
TW0038	Theoretical Computation for a Comprehensive Investigation of Structural Stability, Fracture Toughness, Anisotropic Elasticity, and Thermodynamic Properties of the Copper-Bismuth Binary Intermetallic Compound	Yang-Lun Liu	Feng Chia University

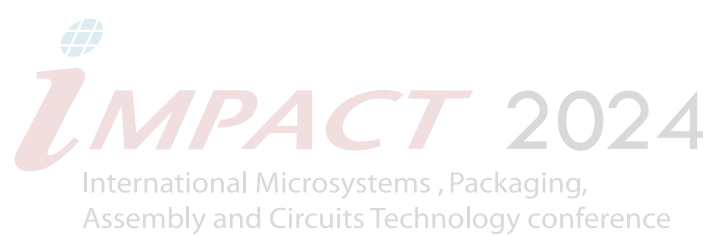
Paper Code	Topic	Lead Author	Affiliation
TW0041	Multi-device and Multi-product Load Rate Analysis Tool under Capital Expenditure	Chun-Wei Hung	Universal Scientific Industrial
TW0096	Solid Solution Effect on the (Bi) Phase	Hsiu-Mei Yang	National Cheng Kung University
TW0116	Applications of high-thermal-conductivity Carbon Nanotubes (CNTs) in TSV applications	Chien-Hao Liu	National Taiwan University
TW0123	A Through Mold Metal Scheme Integrated into In-Molded Electronics Fabrication for Heat Dissipation: Simulation-Based Insights.	Hsu YuLin	Industrial Technology Research Institute (ITRI)
TW0137	Modular Edge Design and Thermal Mechanical Considerations for 5G vRAN and Edge AI	Ming-Wei Tien	Intel Microelectronics Asia LLC Taiwan Branch
TW0148	Design of Microstrip Gap Waveguide Based on Dual-Layer UC-EBG Structure	Ruenn-Bo Tsai	National Sun Yat-sen University (NSYSU)
AS0014	Feasibility Evaluation of Environmentally Friendly Solder Paste with Ultra-low Flux Residue	Chen JunFeng	USI
EU0088	Comparison of through-thickness damage distributions in sheets in bending under tension predicted by several empirical ductile fracture criteria	Marina Rynkovskaya	RUDN University
TW0033	Automatically Generate SMT Mounter Production Data with Python Web Scraping	Chun-Wei Hung	Universal Scientific Industrial
TW0049	Advanced PCI Express Receiver Channel Signal Quality Validation For AI Server	Dian-Ying Wu	Intel
TW0055	High power laser sub-mount of DPC ceramic for Edge Emitting Laser applications	Eric Shen	Tong Hsing Electronic Industries, Ltd.
TW0093	Efficient Management of High-Volume PCB Manufacturing Through Statistical In-board Characterization Analysis	Yu Hsuan Chen	Intel
TW0125	Substantially improved electromagnetic interference shielding performance of gradient-conductive Ti3C2TxMXene/polyimide composite films	Nasima Khatun	National Taipei University of Technology



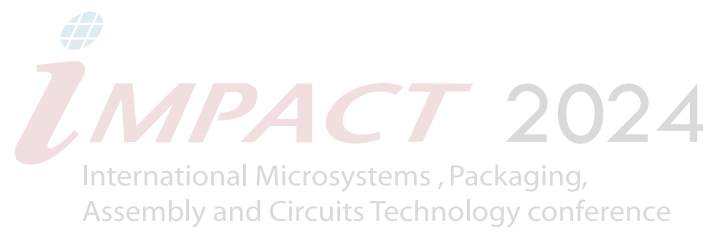
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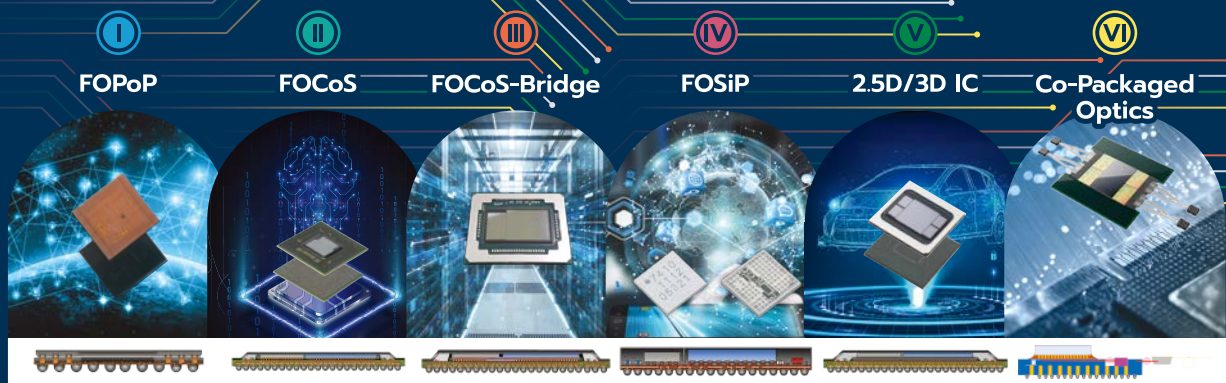
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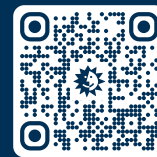
INTEGRATED DESIGN ECOSYSTEM

ASE's integration and miniaturization technologies are enabling transformative solutions that are literally changing lives, from Health to Transportation, from Robotics to AI, and from IoT to 5G.

ASE's VIPack™ is comprised of six core packaging technology pillars supported by an integrated design ecosystem. Please ask the ASE technologists about how we can innovate, collaborate and work together.



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DuPont Material Solutions for IC Substrate

杜邦 IC 載板材料解決方案



應用於mSAP和SAP製程的互連材料

Interconnection materials for mSAP and SAP

杜邦電子互連科技事業部為您帶來業界領先的金屬化藥水和乾膜光阻的整體材料解決方案，協助 IC 載板客戶加速新產品開發，提高生產效率。

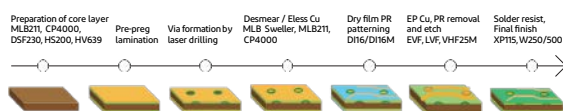
DuPont Interconnect Solutions offers a total solution with industry leading products covering metallization chemicals and dry film photoresist, which helps the IC substrate fabricators to accelerate new product development and improve production efficiency.

價值 Value in Use

- 杜邦™ Circuposit™ 除膠渣和化學銅產品，應用於mSAP和SAP工藝
DuPont™ Circuposit™ desmear & electroless copper for mSAP and SAP processes
- 杜邦™ Copper Gleam™ 導通孔電鍍和通孔填孔電鍍，應用於核心層的電鍍
DuPont™ Copper Gleam™ conformal plating & through hole plating for core layer
- 杜邦™ Microfill™ 盲孔填孔電鍍，應用於mSAP和SAP的增層電鍍
DuPont™ Microfill™ blind via filling for build-up layer
- 杜邦™ Riston® 乾膜光阻用於IC載板的核心層、增層、最終表面處理及銅柱電鍍
DuPont™ Riston® dry film photoresist for core layer, build-up layer, final finish and Cu Pillar

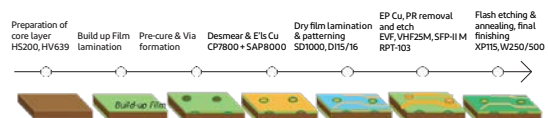
DuPont Solution for FCCSP Substrate, mSAP

Products	Applications
Circuposit™ MLB sweller	desmear
Circuposit™ MLB 211/213	desmear
Circuposit™ 4000	electroless Cu for PTH, mSAP
Copper Gleam™ HS200	conformal plating for core layer – through-hole plating
Copper Gleam™ HV639	conformal plating for core layer – through-hole plating
Microfill™ EVF	microvia filling for substrate build up layer
Microfill™ LVF-IV	via filling for mSAP fine line
Microfill™ VHF25M	microvia filling for fine Line
Microfill™ SFP-II M	microvia filling for fine line with superior uniformity
Riston® DSF230	dry film photoresist for core layer
Riston® DI16/DI16M	direct imaging dry film photoresist for build-up layer, mSAP
Riston® XP115/120	dry film photoresist for gold plating
Riston® W250	dry film photoresist for ENIG
Riston® W500	dry film photoresist for ENEPIG



DuPont Solution for FCBGA Substrate, SAP

Products	Applications
Circuposit™ 7800	SAP desmear for build-up layer; Adv. film, Low Ra.
Circuposit™ SAP8000	SAP electroless Cu for build-up layer, Ionic Pd
Copper Gleam™ HS200	conformal plating for core layer – through-hole plating
Copper Gleam™ HV639	conformal plating for core layer – through-hole plating
Microfill™ EVF	microvia filling for substrate build up layer
Microfill™ VHF25M	microvia filling for fine line & big body size
Microfill™ SFP-II M	microvia filling for fine line and big body size
Microfill™ RPT-103	microvia filling with excellent uniformity at >5 ASD
Riston® SD2000	dry film photoresist for SAP fine line, RDL; Stepper (i-line)
Riston® DI16/DI16M	direct imaging dry film photoresist for build-up layer, SAP
Riston® WBR3000 /4000	dry film photoresist for Cu pillar
Riston® W250	dry film photoresist for ENIG
Riston® W500	dry film photoresist for ENEPIG



應用 Applications

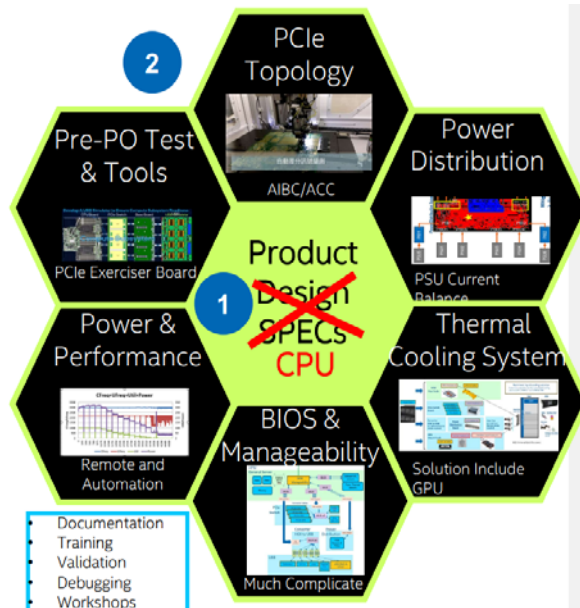
用於FCBGA，FCCSP和SiP/Module載板的先進材料解決方案，廣泛應用於SAP和mSAP工藝

Advanced material solutions for FCBGA, FCCSP and SiP/Module Substrates, widely used in SAP and mSAP processes

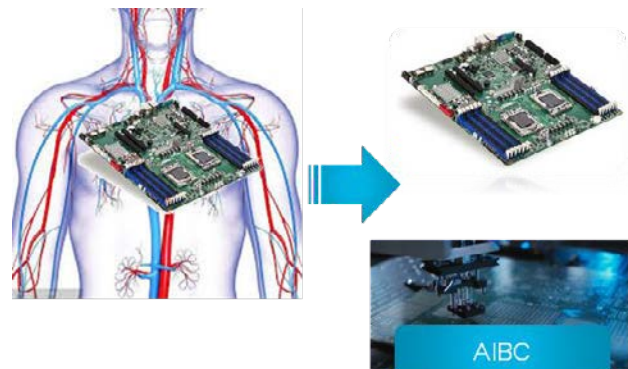
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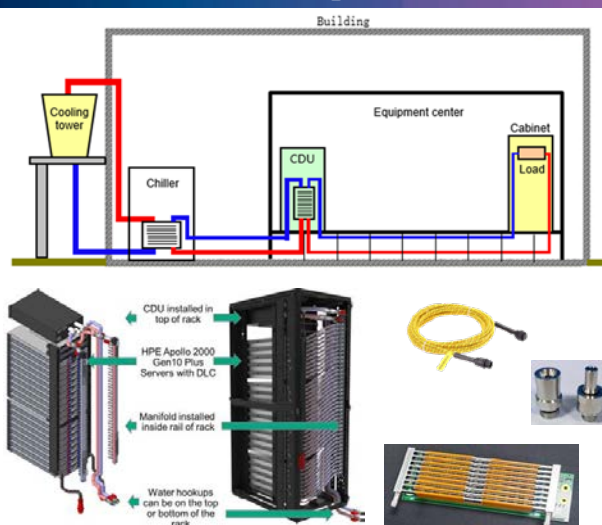
System Architecture of Intel Data Center AI Server Solutions



Intel® Automatic In-board Characterization (AIBC)

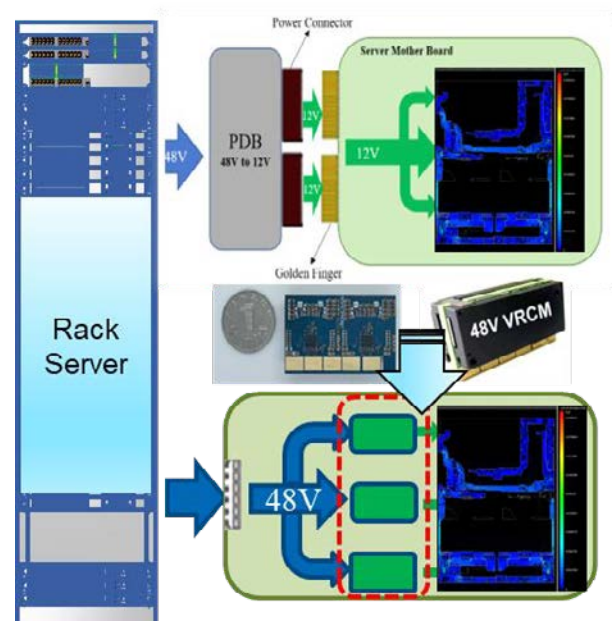


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48V System Power Distribution: Design Challenge Analysis



When differential etching meets complex systems



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With **EcoFlash® S300** – MKS' Atotech continues to raise the performance bar. As a differential etch, EcoFlash® S300 meets the fine line capabilities of < 8/8 L/S for IC substrates while being easy to use, undercut-free, cost-effective, and sustainable. The robust process improves production yield and is ideally suited for ultra-fine line IC substrate manufacturing. Additionally, it comes with lower production and waste-treatment costs thanks to easy solution regeneration. The simple, one-step, and low-temperature process assures a stable and easy-to-control etch rate while improving your environmental footprint.

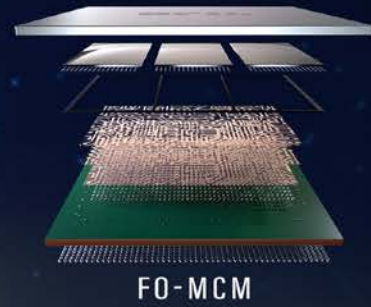
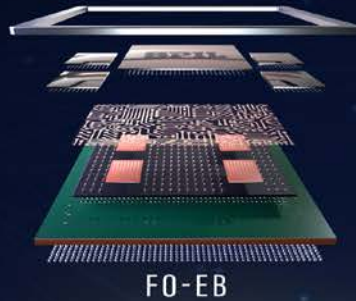
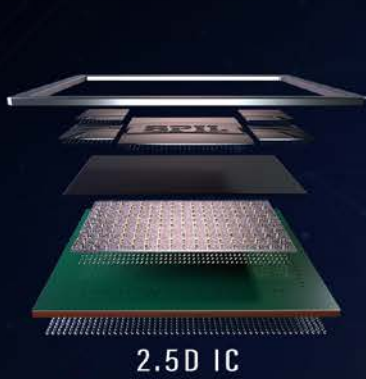
To find out more about EcoFlash® S300, scan the QR-code to the right.



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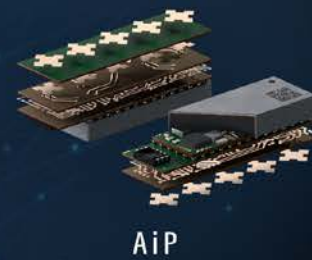
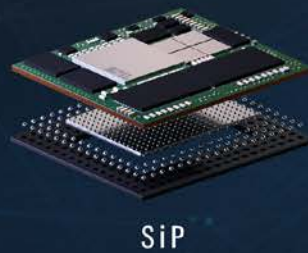
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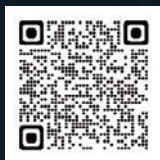


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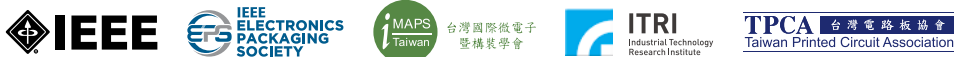
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