3DS IC Test Cost Reduction Challenges

Report by Wendy Chen
The greatest prophet of Semiconductor

Gordon Moore
✓ Fairchild Director of R&D
✓ Co-founder of Intel
✓ Intel CEO and Chairman during (1979~1997)

The technology driving force of Integrated electronics is Reduced Cost
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.”

Electronics, Volume 38, Number 8, April 19, 1965
Topics

- Traditional IC test method overview
- 3DS IC test challenges and potential solution
- The test challenges of next decade 3D IC
- Conclusion
System Level Test:
- IC only was done function test by application board
- Go/ No Go

It was a popular test method by manual test before 1990.
System Level Test

After 2000 SLT became automation and still was popular now

- IC test by application board with auto handler and PC
- Compensate test coverage rate
- Not only Go/ No Go, could separate different level of device’s quality grade
Typical VLSI Test

- DC Parameter Test (Static Test)
- Functional Test
- AC Parameter Test (Dynamic Test)
- Reliability Stress Test
The price of transistor drop down nearly 1 order of magnitude per 4 year.
DESIGN for TEST – SCAN CHAIN

Structural Scan

Combinational Block
Feedback network with m flip-flops

Combinational and Sequential Logic

4-Bit Scan Vector

DIGITAL TEST GENERATION AND DESIGN FOR TEST ABILITY
DESIGN for TEST (DFT)

Structural Scan

- **DC Scan** (Stack At Fault, Bridge Fault, Transition Fault)
- **AC Scan** (Delay Fault)

- Example-Stuck at fault
- Example-Path delay fault

DC Scan

AC Scan
Advantage:

- Easy to localize defect
- Test pattern directly generate from design tool
- Reduce the occupation of expensive tester

Need to find the “sweet spot” of test cost

Disadvantage:

- Additional DFT circuit will increase device unit cost
- Test coverage is not enough
- DFT is not mature on Analogy, PMIC, RF and Sensor
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3DS IC test challenges and potential solution

What is testing difference between SIP and 3DS IC?
The Trend of IC Structure

Cost function vs. time to market vs. System complexity

SOC, SIP, 3D, POP, PiP

KGD/PGD approach
What is testing difference?

SOC
- Defect Mode
- Functional Test
- DFT / BIST
- EDA
- Data Mining
- Probe access point
- Wafer handling
- KGD/PGD
- Burn In
- Supply Chain

POP/PIP
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3DSIC
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Options:
- Don’t need
- Portion
- Same
- Enhance
- New
3DS IC New Defect mode

- **Faults came from in TSV itself**
  - Voids (High resistance)
  - Oxide pinholes (short to substrate)

- **Faults came from bonding**
  - Contamination of bond surface
  - Misalignment
  - Height Variation
  - Signal connection (TSV or micro-bump/ short, open or poor contact)

- **Faults came from wafer thinning**
  - Non properly release stress to impact device’s performance
  - Micro crake during wafer thinning process
  - Micro crake during thin wafer probing
3DS IC DFT Challenges

- Structural Scan: Not only 2D, need increase to 3D
- AC Scan: Delay Faults, Small Delay Faults are good for detect TSV performance and layer to layer timing variation

The small delay fault is good for detect 3DS performance
But
The length of scan vector will increase dramatically and also need precise timing resolution

<table>
<thead>
<tr>
<th>Fault Type</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAT (Stuck At Fault)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>BF (Bridging Fault)</td>
<td>1.3</td>
<td>1.3</td>
</tr>
<tr>
<td>TF (Transition Fault)</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>SD (Small Delay)</td>
<td>2</td>
<td>40</td>
</tr>
</tbody>
</table>

Source from ITRS 2010 Test table of DFT
EDA Challenges

- **Floor planning**
  - Partition blocks into different dies
  - Connectivity

- **Timing**
  - TSV characteristics (RLC)
  - Timing clock tree
  - Variation of timing due to multiple wafer process technologies

- **IR Drop**
  - Power sources of connected power domains are shared
  - Longer routing lengths + TSV

- **Parasitic Extraction**
  - Different stacking schemes have different impact on parasitic extraction
  - Noise coupling effects

- **Thermal Analysis**
  - Thermal extraction of bonding layers
  - Thermal model correct to real process.

Source: from Mentor Graphic
BIST Potential solution

- DRAM Die
- Wide I/O TSV Bus
- Multiple SoCs (with DFT)
- TSV Interconnect
- I/O to outside

BIST for Stacked DRAM & Wide IO

BIST & ATPG compression for in-package die test

Hierarchical ATPG for TSV test
Data Mining & potential solution

EDA

Databases & Automated Data Analysis
(This may include multiple databases. ‘Analysis’ includes capabilities like post-test statistical analysis, dynamic routings and feedforward data.)

• Fab data
• Design data
• Business data
• Customer specs

Assembly Operations
(This includes test operations at any level of assembly.)

Test Cell

Die Stacking

Analysis

Yield Issue!

Test Cell

Pass / Fail

Rejected Units

Good Units

RT A/O

“RT A/O” stands for “Real-Time Analysis & Optimization”

PTAD

“PTAD” is “Post-Test Analysis & Dispositioning”

Source from ITRS 2011 Test edition
Thin wafer handling

Ideal KGD required probe thin wafer before grinding

Prober capability limitation:
- 12’ prober handle thin wafer capability > 6 mil
- 8’ prober handle thin wafer capability > 4 mil

Potential solution
- Frame prober solution
- Novel process: Taiko grinding wafer.

Cost consideration, Probing wafer before grinding or probing wafer after WTW bond.
Supply Chain Model

- The decision of Co-Design and supply chain became importance in the design stage.
- System maker will become major design ownership for 3DS IC in the future.
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Evolution of 3D IC

We are discussing topic

KYEC already done mass production test

Source from ASE
Beyond the year 2022

3DS IC Heterogeneous integration

Optical communication > 40Gbps

Atom transistor

MEMS sensor

Bi-computing

Courtesy of European Nanotechnology Roadmap
Beyond the year 2022

Test challenges

- KGD/PGD requirement might change to KGC/PGC (cube).

- Generate complexities of stimulation test signal input
  Heterogeneous Integration 3DS IC.

- New material (optical waveguide, bio-network…) challenge DFT technology and EDA tool design.

- The investment of new accessories and equipments will increase test cost
Conclusion

- TSV process was mature and will continually dominate 3DS IC interconnect over next decade.

- Probing TSV only for engineering analysis, not suitable for mass production from test cost consideration.

- DFT, BIST/BISR/BISD and Data Mining are very important test technology for 3DS IC testing.

- 3DIC EDA development and test protocol standardization could enhance test quality and reduce test cost.
- Testing is necessary Evil
- Zero Defect is Manufacturing Dream
- Cost Reduction drive Innovative Technology